THE GIGABIT SWITCH (WUGS-20) LINK INTERFACE SPECIFICATION

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1 Overview

This document serves as the technical specification for adapter cards designed to operate with the latest version of the Washington University Gigabit Switch (WUGS-20). The Gigabit Switch has eight (8) link interfaces that reside on adapter cards that connect with the main switch board via controlled-impedance connectors. The use of interchangeable adapter cards allows several types of link interfaces to be supported, including 622 Mb/s or 1.2 Gb/s Hewlett-Packard G-Link [1], 2.4 Gb/s G-Link, 155 Mb/s SONET, 622 Mb/s SONET, and 2.4 Gb/s SONET. The 2.4 Gb/s G-Link link interface is supported using two, parallel 1.2 Gb/s G-Link subsystems on a single adapter card.

On the main switch board, each adapter card interface is implemented using an Output Port Processor (OPP) and an Input Port Processor (IPP). The OPP and IPP are custom Integrated Circuits (ICs) that supply ATM cells to an adapter card for transmission and accept received ATM cells from an adapter card, respectively. The OPP and IPP use a subset of the functionality defined in the *Universal Test & Operations PHY Interface for ATM* (UTOPIA) [2] standard in order to simplify link interface design. TTL signal levels are used on the interface.

The OPP and IPP operate in either 16-bit or 32-bit mode as defined by an option pin on each IC. In 16-bit mode, the cell format defined by the UTOPIA standard [2], which is compatible with the PMC-Sierra PM5345 [3], the PM5348 [4], and the PM5355 [5] Saturn User Network Interfaces (SUNIs), is used. The 16-bit mode supports transmission at rates up to 1.2 Gb/s. In 32-bit mode, a simple extension of the 16-bit UTOPIA interface is used. The 32-bit mode supports transmission at rates up to 2.4 Gb/s.

To minimize signal reflection at the physical connector and support the maximum possible clock and data rates, the main switch board uses 61 Ohm traces (61 Ohms +/- 7 Ohms) between the OPP and IPP and the controlled impedance connector. Signals driven by the OPP and IPP are source terminated at the IC. It is recommended that all adapter cards use 61 Ohm traces between the physical connector and the terminating ICs and that all signals driven across the connector by an adapter card be source terminated using an appropriate series resistor. Where necessary, signals have been duplicated at the OPP and IPP so that signals between the main switch board and adapter cards can run point-to-point; thus, source termination is an acceptable termination scheme.

The main switch board has been designed to operate without link interface adapter cards. OPP and IPP inputs and clocks are pulled either high or low on the main switch board using 10 KOhm pull-up/pull-down resistors. The use of pull-ups and pull-downs on the main switch board allows adapter cards to ignore many unused signals and treat them as no-connects.

2 The OPP Interface

The OPP signals used by a link interface adapter are shown in Figure 1 along with a timing diagram illustrating operation of the OPP interface. The signal at each pin is defined below. The equivalent UTOPIA signal name is identified where appropriate.

The OPP implements the UTOPIA transmit interface with cell-level flow control. For 32-bit operation, a simple extension of the 16-bit data path is used. The OPP has been designed to "fly-wheel," i.e., it operates with cell cycle periods of either 27 or 14 clock periods, with a cell transmission beginning at the start of a cell cycle or not at all. In 16-bit mode, a cell cycle is 27 clock periods; in 32-bit mode, a cell cycle is 14 clock periods. The cell transmitted to the link interface by the OPP is complete, including a newly computed HEC byte.

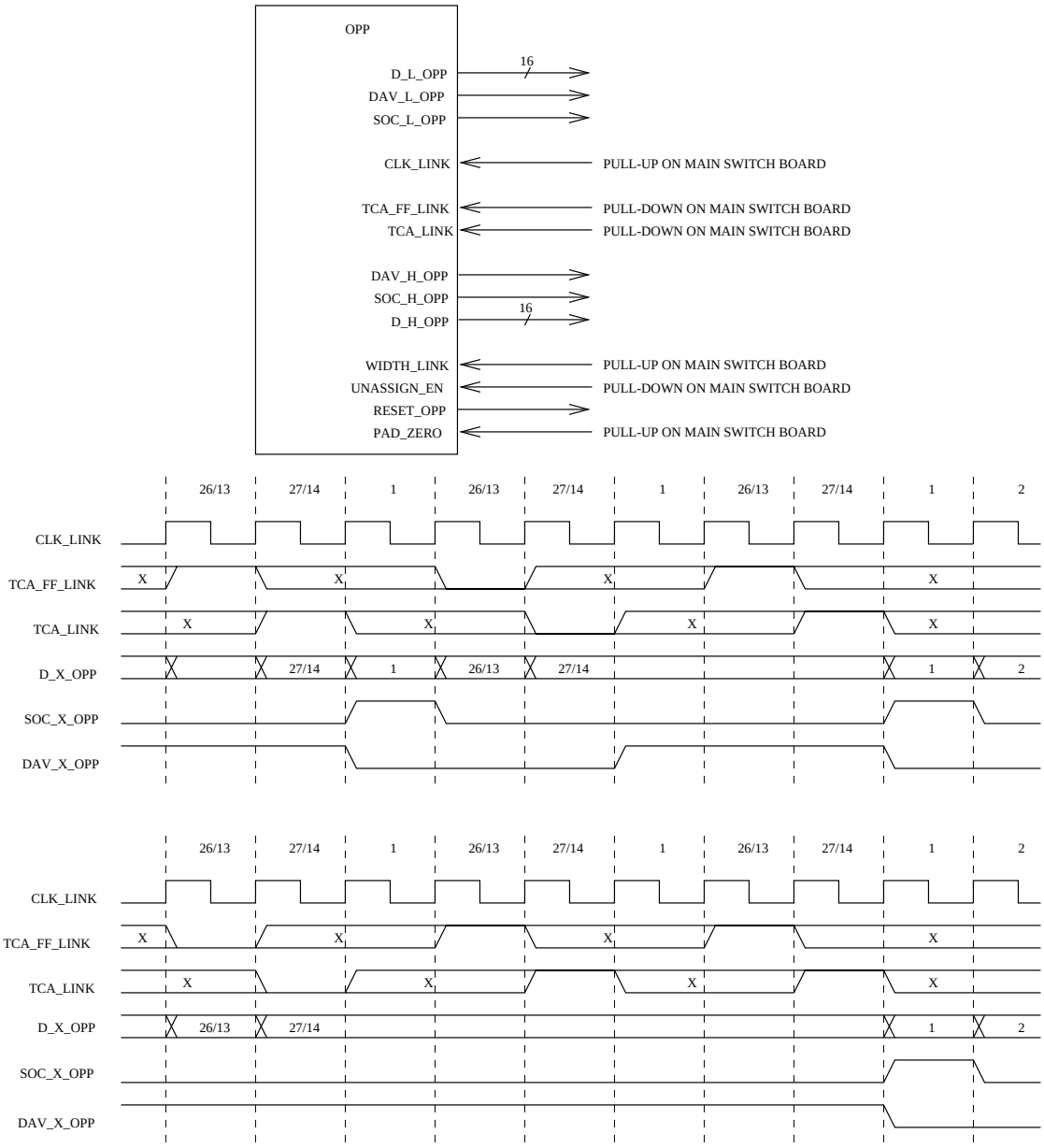


Figure 1: The Output Port Processor (OPP)

WIDTH_LINK

The WIDTH_LINK signal, supplied by the adapter card to both the OPP and the IPP, determines the width of the data path used by the OPP and the IPP; a logic zero on this pin specifies use of the 16-bit mode. This signal has a 10 KOhm pull-up on the main switch board. Link interface adapters using the 16-bit mode must pull this signal to a logic zero; WIDTH_LINK is not allowed to change after reset. This signal is the only signal defined on the link interface adapter connector that goes to more than one IC pin on the main switch board (is not point-to-point).

UNASSIGN_EN

The UNASSIGN_EN signal, supplied by the adapter card, indicates that unassigned cells should be transmitted by the OPP when a valid data cell is not available for transmission. The table in Figure 2 describes the

Link Ready to Accept Another Cell?	OPP Has A Cell Ready to Send?	UNASSIGN_EN	OPP Sends...
NO	Does Not Matter	Does Not Matter	No Cell
YES	YES	Does Not Matter	The Cell That Is Ready
YES	NO	Logic 0	No Cell
YES	NO	Logic 1	Unassigned Cell

Figure 2: Table Defining UNASSIGN_EN Operation

behavior of the OPP chip. The link is ready to accept another cell if TCA_FF_LINK is asserted high at the proper time, or if the WIDTH_LINK signal indicates 16-bit mode and TCA_LINK is asserted high at the proper time (see the descriptions of TCA_LINK and TCA_FF_LINK for the proper times), or both. The OPP sending "no cell" means that the appropriate SOC signal(s) will remain low, and the appropriate DAV signal(s) will remain high, for one cell time.

The UNASSIGN_EN signal has a 10 KOhm pull-down on the main switch board. Link interface adapters requiring unassigned cells must pull this signal to a logic one; UNASSIGN_EN is not allowed to change after reset.

The unassigned cell transmitted by the OPP when UNASSIGN_EN is asserted is a cell with all 52 non-HEC bytes equal to zero (HEC = 55H), i.e., the CLP bit is set to zero. This cell differs from the IDLE cell; IDLE cells have the CLP bit set to one.

CLK_LINK (UTOPIA: TxClk)

The OPP link interface clock, CLK_LINK, is provided by the adapter card. The OPP link interface is designed to operate at clock rates up to 80 MHz. The minimum high and low times for this signal are 4 ns. The minimum clock period is 12.5 ns; the maximum rise time is 7 ns. This signal has a 10 KOhm pull-up on the main switch board.

Adapter cards must be designed so that connecting or disconnecting a fiber does not result in the minimum high time, the minimum low time, or the minimum period of CLK_LINK being violated.

D_L_OPP (UTOPIA: TxData[15:0]) and D_H_OPP

The D_L_OPP and D_H_OPP signals implement the 16- or 32-bit data path between the OPP and the link interface adapter. In 16-bit mode, only the D_L_OPP signals are used, and the operation of the D_H_OPP signals is undefined. In 32-bit mode, the D_L_OPP and D_H_OPP signals are used to form the 32-bit-wide data path between the OPP and the link interface adapter. These signals are synchronous with CLK_LINK. See Figure 10 for the clock-to-output times.

DAV_L_OPP and DAV_H_OPP (UTOPIA: TxEnb*)

The DAV_L_OPP and DAV_H_OPP signals supplied by the OPP are the (true low) write enable signals for the two 16-bit portions of the OPP data path. In 32-bit mode, DAV_H_OPP will be identical to DAV_L_OPP; it is supplied so that point-to-point wiring from the OPP to the adapter card circuitry is possible. For adapter cards that implement a single 32-bit data path, either signal may be used. In 16-bit mode, the operation of the DAV_H_OPP signal is undefined. These signals are synchronous with CLK_LINK. See Figure 10 for the clock-to-output times.

SOC_L_OPP and SOC_H_OPP (UTOPIA: TxSOC)

The (true high) SOC_L_OPP and SOC_H_OPP signals supplied by the OPP are used to identify the first word of an ATM cell. In 32-bit mode, SOC_H_OPP will be identical to SOC_L_OPP; it is supplied so that point-to-point wiring from the OPP to the adapter card is possible. For adapter cards that implement a single 32-bit data path, either signal may be used. In 16-bit mode, the operation of the SOC_H_OPP signal is undefined. These signals are synchronous with CLK_LINK. See Figure 10 for the clock-to-output times.

TCA_LINK and TCA_FF_LINK (UTOPIA: TxClav)

The TCA_LINK and TCA_FF_LINK signals supplied by an adapter card are used to signal the ability of the adapter card to accept another cell. Only one of these two signals is used by any given adapter card. The OPP has been designed to "fly-wheel," i.e., it operates with cell cycle periods of either 27 or 14 clock (CLK_LINK) periods, with a cell transmission beginning at the start of a cell cycle or not at all. In 16-bit mode, a cell cycle is 27 clock periods; in 32-bit mode, a cell cycle is 14 clock periods. TCA_FF_LINK is latched by the OPP at the end of clock period 26 of a 27 clock period cycle (16-bit mode) or at the end of clock period 13 of a 14 clock period cycle (32-bit mode). Most UTOPIA devices will assert a Transmit Cell Available (TxClav) signal high at least four (4) clock cycles before the end of a cell cycle if the device can accept an additional cell immediately after completion of the transfer of the current cell. The OPP is designed so that, even though the TCA_FF_LINK signal may be asserted early by a UTOPIA device, TCA_FF_LINK must *only* meet the specified set-up and hold times relative to the rising edge of the OPP clock (CLK_LINK) at which it is latched internally. The set-up and hold times of TCA_FF_LINK, at the OPP, are specified in Figure 11.

TCA_FF_LINK has a 10 KOhm pull-up resistor on the main switch board. When the TCA_LINK signal is used instead of the TCA_FF_LINK signal, the TCA_FF_LINK signal must be pulled low by the adapter card. The default state of TCA_FF_LINK is, therefore, asserted; this assures that OPP will "drain" cells destined for a link if no link adapter card is used. While not draining cells in the current switch is not seen as a problem, it could be with future switches that flow control back to the fabric. This definition represents a change from Version 4.1 of this document, and 155 Mb/s SONET cards designed to use the TCA_LINK signal will need to pull the TCA_FF_LINK signal low (whereas it could be ignored previously).

The TCA_LINK signal is supplied to allow operation with early 16-bit UTOPIA devices that assert TCA during the last clock period (word transfer) of a cell cycle, e.g., the PMC-Sierra PM5345. TCA_LINK is masked out and not used by the OPP in 32-bit mode. This signal is not latched internal to the OPP, and the set-up time, at the OPP, is specified as 10 ns. The maximum clock rate (CLK_LINK) is 25 MHz when TCA_LINK is used. The hold time is specified as 0.0 ns. This signal is buffered and used directly by the internal FSM to determine whether or not a new cell will be transmitted during the next cell cycle. TCA_LINK has a 10 KOhm pull-down resistor on the main switch board. For UTOPIA-based designs that assert TCA early, the TCA_LINK signal can be ignored and not driven. In this case, the TCA_FF_LINK signal should be used instead of the TCA_LINK signal. (Note: Future versions of the OPP will not support the TCA_LINK signal, and new adapter card designs should use the TCA_FF_LINK signal.)

RESET_OPP

The RESET_OPP signal is a buffered reset signal produced by the OPP at power-up, in response to the switch reset push button, or in response to a software-generated reset. This signal is active low and its assertion (falling) edge is asynchronous to CLK_LINK, while its deassertion (rising) edge is synchronous to CLK_LINK, using the circuit shown in Figure 3. The RESET signal synchronized to the switch fabric clock CLK is driven

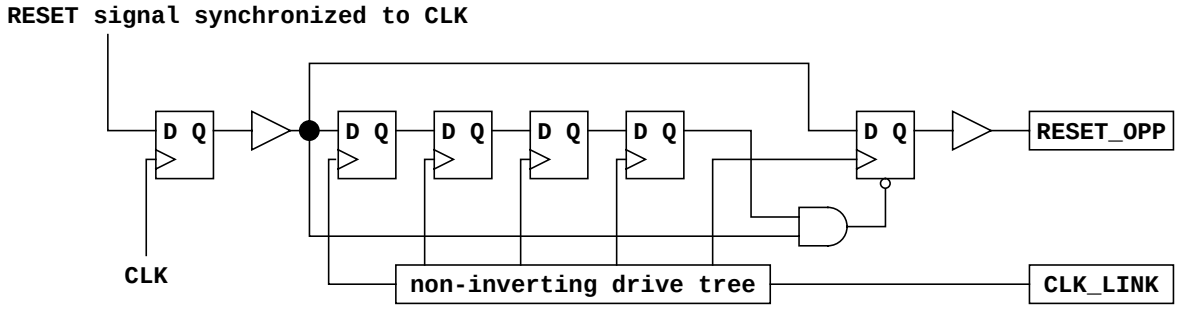


Figure 3: Circuit Used to Drive RESET_OPP Output

on the main board from a debouncing circuit that guarantees that it remains low for at least 0.5 ms. See Figure 10 for the clock-to-output times for the deassertion (rising) edge.

Note that it is possible for RESET_OPP to go low twice in response to RESET going low once, but this could only happen if 4 CLK_LINK periods lasted longer than RESET was low, i.e., CLK_LINK frequency is less than 8000 Hz.

PAD_ZERO

The PAD_ZERO signal is a new signal that was not included prior to version 5.0 of this technical report. PAD_ZERO is an input to the OPP. When PAD_ZERO is high, cells transmitted by the OPP will have the UNUSED/ZERO and UNUSED/LINKINFO bytes (see Figure 7 and Figure 8 in a later section) set to zero as required by UTOPIA devices. This was the mode of operation defined prior to the introduction of the PAD_ZERO signal.

When the PAD_ZERO signal is low, however, cells transmitted by the OPP will have the UNUSED/LINKINFO byte filled with additional information required by future adapter cards. The format of this byte is shown in Figure 4. The contents of the 4 bit LINK_INFO field are actually filled in by the last IPP chip that the cell

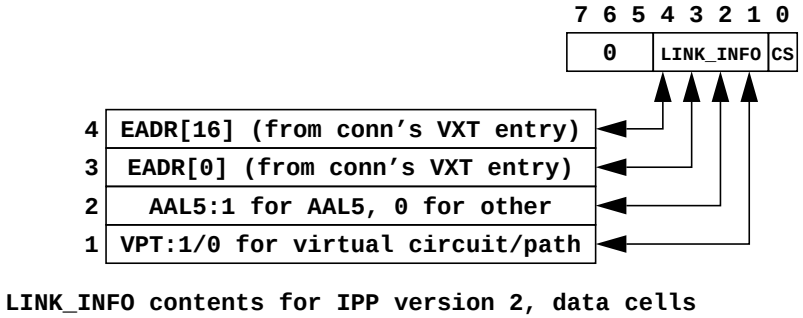


Figure 4: Contents of LINKINFO byte when PAD_ZERO is low

passed through before reaching the OPP and being forwarded to the adapter card. That OPP merely propagates or zeros out that information depending on the value of its PAD_ZERO input pin.

For IPP version 1, LINK_INFO is not filled in with useful information: the most significant 4 bits of the 16 bit Source Trunk Group (STG) field for data cells, and unknown for control cells. See [6] for definitions of the STG, EADR, VPT, and CS fields. For IPP version 2, LINK_INFO is filled in as shown in Figure 4 for data cells. Control cells can specify the contents of their own LINK_INFO bits by a field of the same name within their payload. See [6] for the location of this control cell field.

If UNASSIGN_EN is asserted high, so that unassigned cells are transmitted by the OPP, the UNUSED/ZERO and UNUSED/LINKINFO bytes of the unassigned cells will always be filled with zeros, regardless of the value of PAD_ZERO.

The PAD_ZERO signal has a 10 KOhm pull-up resistor on the main switch board. Adapter cards that do not need the additional information contained in the UNUSED/LINKINFO byte can therefore ignore and not drive this signal.

3 The IPP Interface

The IPP signals used by a link interface adapter are shown in Figure 5 along with a timing diagram illustrating operation of the interface. The signal at each pin is defined below.

The IPP implements the UTOPIA receive interface without the need for octet-level or cell-level flow control. The IPP is designed to accept a continuous stream of ATM cells. This ability allows the IPP to accept ATM cells as soon as they are available-no buffering on the adapter card is required. Once the start of a cell transfer is signaled via assertion of the appropriate start-of-cell signal(s), the link interface adapter must supply that cell without interruption. This mode of operation is supported by the UTOPIA standard via continuous assertion of the RxEnb* signal.

For 32-bit operation, a simple extension of the 16-bit data path is used. The IPP does not normally require that link interface adapters "fly-wheel," i.e., operate with either 27 or 14 clock periods per cell cycle, with a cell transmission beginning at the start of a cell cycle or not at all. The one exception to this is that 32-bit link interface adapters using the de-skewing circuitry inside the IPP to compensate for clock and data skew across separate 16-bit data buses must flywheel; 14 clock periods per cell cycle must be used with cell transmission beginning in the first clock period or not at all.

The IPP is designed to check the HEC byte supplied by the link interface adapter; a valid HEC byte must be transmitted to the IPP by the link interface adapter for a cell to be recognized as a valid ATM cell.

WIDTH_LINK

The WIDTH_LINK signal, supplied by the adapter card to both the OPP and the IPP, determines the width of the data path used by the OPP and the IPP; a logic zero on this pin specifies use of the 16-bit mode. This signal has a 10 KOhm pull-up on the main switch board. Link interface adapters using the 16-bit mode must pull this signal to a logic zero; WIDTH_LINK is not allowed to change after reset. This signal is the only

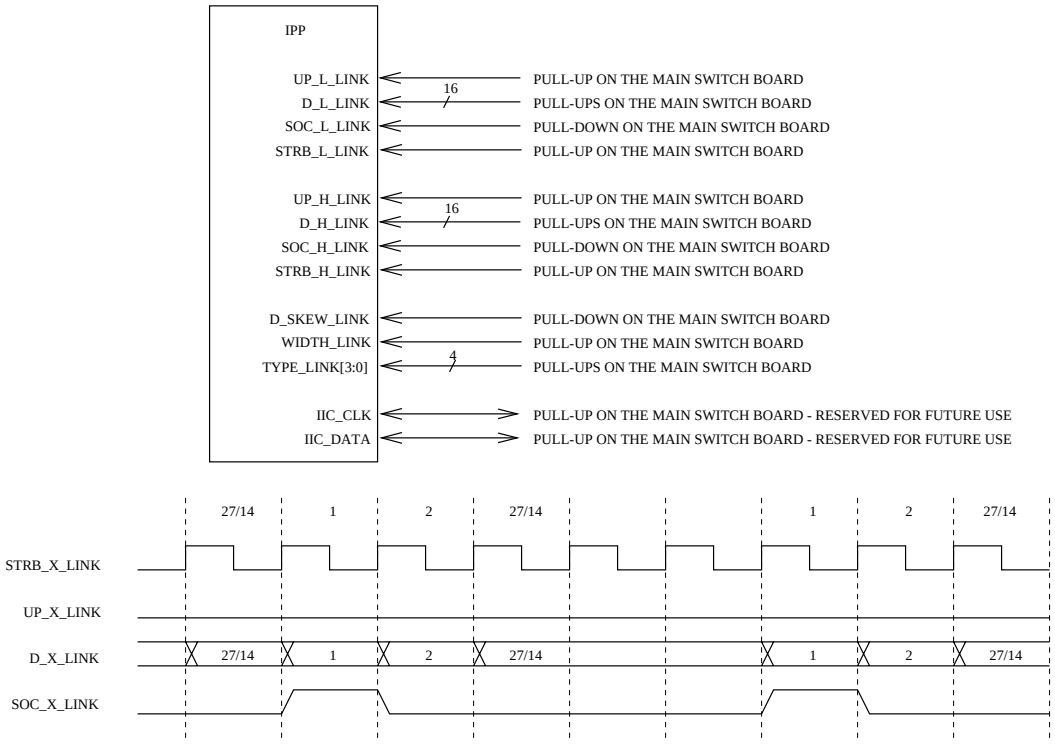


Figure 5: The Input Port Processor (IPP)

signal defined on the link interface adapter connector that goes to more than one IC pin on the main switch board (is not point-to-point).

TYPE_LINK

The four (4) TYPE_LINK signals, supplied by the adapter card, are used to specify the type of link interface implemented by the adapter card. The adapter types currently defined are:

TYPE_LINK[3:0] (hexadecimal)	Type of Link Interface
0	Reserved
1	155.52 Mb/s SONET
2	622.08 Mb/s SONET
3	2.48832 Gb/s SONET
4	625 Mb/s G-LINK
5	1.25 Gb/s G-LINK
6	2.5 Gb/s Double G-LINK
7	Future Expansion
8	Future Expansion
9	Dual 155.52 Mb/s SONET
A	Future Expansion
B	Future Expansion
C	Future Expansion
D	Future Expansion
E	Future Expansion
F	Reserved; No Link Interface

Figure 6: TYPE_LINK codes

TYPE_LINK[3:0] = FH is used to identify OPPs and IPPs that do not have associated link interface circuitry, and the main switch board supplies 10 KOhm pull-up resistors on these signals so that the switch can operate without adapter cards. For future flexibility, it is recommended that adapter cards implement the TYPE_LINK signals using either DIP switches or jumpers. These signals must be tied to either a logic zero or not driven by the adapter card; they are not allowed to change after reset.

STRB_L_LINK and STRB_H_LINK (UTOPIA: RxClk)

The STRB_L_LINK signal is a free-running clock supplied by the link interface adapter card. This clock signal is used to strobe the lower 16 data bits, D_L_LINK, and the SOC_L_LINK signal into the IPP. The minimum high time for this signal is 4 ns; the minimum low time is also 4 ns. The minimum clock period is 12.5 ns; the maximum rise time is 7 ns. STRB_L_LINK has a 10 KOhm pull-up resistor on the main switch board.

The STRB_H_LINK signal is a free-running clock supplied by the link interface adapter card. This clock signal is used to strobe the upper 16 data bits, D_H_LINK, and the SOC_H_LINK signal into the IPP. The minimum high time for this signal is 4 ns; the minimum low time is also 4 ns. The minimum clock period is 12.5

ns; the maximum rise time is 7 ns. STRB_H_LINK has a 10 KOhm pull-up resistor on the main switch board. In 16-bit mode, this signal can be ignored and not driven.

Adapter cards must be designed so that connecting or disconnecting a fiber does not result in the minimum high time, the minimum low time, or the minimum period of STRB_L_LINK or STRB_H_LINK being violated.

Adapters using a single 32-bit data path for the transmission of ATM cells will typically transfer data using a single clock. In this case, the clock must be supplied to both STRB_L_LINK and STRB_H_LINK. Let T_H be the time of the rising edge of STRB_H_LINK that causes the IPP to latch the high 16 bits of some word of a cell. Let T_L be the time of the rising edge of STRB_L_LINK that causes the IPP to latch the low 16 bits of the same word of the same cell. Let T_P be the period of the clock signal that drives both STRB_H_LINK and STRB_L_LINK. Then the constraint -2.0 ns < T_H-T_L < T_P - 10.0 ns must be satisfied. This is the constraint when D_SKEW_LINK is deasserted low.

Separate clock signals are implemented by the IPP to support transmission of 32-bit mode cells over two independent transmission channels using 16-bit data paths where more significant clock (and data) skew at the receiver is possible, e.g., parallel 1.2 Gb/s G-Links implementing a 2.4 Gb/s link (see the design example in Section 6.6). The IPP has special circuitry to compensate for this skew. The constraint -T_P < T_H-T_L < T_P must be satisfied. This circuitry is activated by asserting the D_SKEW_LINK signal high.

Regardless of the level of D_SKEW_LINK, D_L_LINK and SOC_L_LINK must satisfy set up and hold requirements relative to STRB_L_LINK, and D_H_LINK and SOC_H_LINK must satisfy set up and hold requirements relative to STRB_H_LINK. These are given in Figure 11.

D_SKEW_LINK

The D_SKEW_LINK signal, supplied by the adapter card, enables the de-skewing circuitry inside the IPP when it is tied to a logic 1. The level of this signal is only significant for the 32-bit mode. The D_SKEW_LINK signal has a 10 KOhm pull-down resistor on the main switch board. For 16-bit link interface adapters and 32-bit adapters that do not use the de-skewing circuitry, this signal can be ignored and not driven. This signal is not allowed to change after reset.

D_L_LINK (UTOPIA: RxDATA[15:0]) and D_H_LINK

The D_L_LINK and D_H_LINK signals implement the 16- or 32-bit data path between the IPP and the link interface adapter. Both sets of data signals have 10 KOhm pull-ups on the main switch board. In 16-bit mode, only the D_L_LINK signals are used, and the D_H_LINK signals can be ignored and not driven. In 32-bit mode, the D_L_LINK and D_H_LINK signals are used to form the 32-bit-wide data path between the link interface adapter and the IPP.

The set-up and hold times of the D_L_LINK signals relative to STRB_L_LINK, at the IPP, are specified in Figure 11.

The set-up and hold times of the D_H_LINK signals relative to STRB_H_LINK, at the IPP, are specified in Figure 11.

SOC_L_LINK and SOC_H_LINK (UTOPIA: RxSOC)

The (true high) SOC_L_LINK signal, supplied by the adapter card, is used to identify the first word of a cell on the lower 16 data lines, D_L_LINK. It must be asserted coincident with the first word of the cell. The SOC_L_LINK signal has a 10 KOhm pull-down on the main switch board.

The set-up and hold times of the SOC_L_LINK signal relative to STRB_L_LINK, at the IPP, are specified in Figure 11.

The (true high) SOC_H_LINK signal, supplied by the adapter card, is used to identify the first word of a cell on the upper 16 data lines, D_H_LINK, in 32-bit mode when de-skewing is enabled. It must be asserted coincident with the first word of the cell. The SOC_L_LINK signal has a 10 KOhm pull-down on the main

switch board. In the 16-bit mode, and in 32-bit mode when de-skewing is not enabled, SOC_H_LINK can be ignored and not driven.

The set-up and hold times of the SOC_H_LINK signal relative to STRB_H_LINK, at the IPP, are specified in Figure 11.

UP_L_LINK and UP_H_LINK

The UP_L_LINK and UP_H_LINK signals are used by the adapter card to indicate the presence of an optical carrier, or, in the case of SONET transmission, the establishment of valid SONET frame recovery. Two signals are provided so that additional circuitry is not needed on the adapter card when a 32-bit channel is implemented using parallel, 16-bit transmission systems, e.g., when parallel G-Links are used. Both signals have 10 KOhm pull-up resistors on the main switch board. In 16-bit mode, and in 32-bit mode when de-skewing is not enabled, the UP_H_LINK signal can be ignored and not driven.

When UP_L_LINK is not asserted low (in 16-bit mode and in 32-bit mode when de-skewing is not enabled), the IPP ignores cells at its input, i.e., cells are not accepted. When UP_L_LINK and UP_H_LINK are not asserted low (in 32-bit mode when de-skewing is enabled) the IPP ignores cells at its input, i.e., cells are not accepted.

The UP_L_LINK and UP_H_LINK signals are synchronized by the IPP; they are not, therefore, required to be synchronous with the STRB_L_LINK and STRB_H_LINK strobes and can be connected directly to the output of the optical device or SONET subsystem. The signals are asserted true low, i.e., a logic zero indicates that the link is operational (up).

IIC_CLK and IIC_DATA

The IIC_CLK and IIC_DATA signals are not supported by the present IPP. These signals will provide a low data rate serial communication path between adapter cards and the ATM control cell stream. It is expected that this data path would be used by an ATM network control processor to set up and poll PHY interface devices on the adapter cards. These two signals, which will be supported in the next version of the Washington University Gigabit Switch IPP circuit, will follow the Philips Semiconductor "I^2C" Bus [9] specification. Following this specification will allow the use of over 150 different kinds of semiconductor interface devices to be used on the adapter cards. These devices range from an eight bit I/O port to a 68000-based microcontroller. (Note: The main switch board has 10 KOhm pull-up resistors to 5.0 Volts on each of these two signals.)

Initialization/Reset

Read the description of the RESET_OPP signal in Section 2 for information on the duration and synchronization of this signal.

If a link adapter requires a longer reset signal, it must be generated using the supplied reset signal and/or at power-up using special circuitry. The OPP is designed so that SOC_L_OPP and SOC_H_OPP are not asserted while RESET_OPP is asserted low. These signals will be asserted once per cell cycle after this initial reset period if the OPP is strapped to send unassigned cells and the transmit cell available signal (either TCA_FF_LINK or TCA_LINK) is asserted.

At power-up, in response to the switch reset push button, or in response to a software-generated switch reset, the IPP is designed to ignore input data for 2^{20} switch fabric cell times, or 2^{24} switch fabric clock cycles (about 0.14 sec if the switch fabric clock is running at 120 MHz). During this time, the link adapter circuitry can supply erroneous data (invalid cells) to the IPP. Since cells cannot enter the switch for this 2^{24} switch fabric clock cycle period, it is impossible for OPPs to have valid data cells to transmit to the link interface adapters during this period. Link adapters can use this period to program registers, etc., to support ATM cell transmission.

4 Cell Format Definition

The 16-bit cell format used by the gigabit switch is shown in Figure 7. This cell format is compatible with that specified by Version 2.01 of the UTOPIA standard [2]. The OPP supplies the HEC byte and a zero byte as the third word during transmission. The IPP expects to receive the HEC byte in the third word of received cells. The non-HEC byte in the third word is ignored by the IPP.

The 32-bit cell format used by the gigabit switch is shown in Figure 8. This cell format is an extension of the 16-bit UTOPIA cell format. The OPP supplies the HEC byte and three (3) zero bytes as the second word during transmission. The IPP expects to receive the HEC byte in the second word of received cells. The non-HEC bytes in the second word are ignored by the IPP.

The cell format given above is valid in all cases when the new PAD_ZERO signal is high. When the PAD_ZERO signal is low, however, cells transmitted by the OPP will have the UNUSED/LINKINFO byte filled with additional information required by future adapter cards (see the definition of PAD_ZERO for a complete description of operation in this mode).

	15	0
0	HEADER 1	HEADER 2
1	HEADER 3	HEADER 4
2	HEC	UNUSED/LINKINFO
3	PAYLOAD 1	PAYLOAD 2
4	PAYLOAD 3	PAYLOAD 4
	...	...
	...	...
	...	...
26	PAYLOAD 47	PAYLOAD 48

Figure 7: Cell Format, 16-bit Mode

	31			0
0	HEADER 1	HEADER 2	HEADER 3	HEADER 4
1	HEC	UNUSED/ZERO	UNUSED/ZERO	UNUSED/LINKINFO
2	PAYLOAD 1	PAYLOAD 2	PAYLOAD 3	PAYLOAD 4
3	PAYLOAD 5	PAYLOAD 6	PAYLOAD 7	PAYLOAD 8
	...	...	...	...
	...	...	...	...
	...	...	...	...
13	PAYLOAD 45	PAYLOAD 46	PAYLOAD 47	PAYLOAD 48

Figure 8: Cell Format, 32-bit Mode

5 OPP and IPP Timing and Electrical Characteristics

5.1 OPP and IPP Timing Information Summary

The timing information shown in Figure 9, 10, and 11 below pertains to the OPP and IPP. These values do not take the Printed Circuit Board (PCB) or connector into account; allowance should be made for both where appropriate.

Clock	Min High/Low	Max Rise	Min Period	Unit
CLK_LINK	4/4	7	12.5	ns
STRB_L_LINK	4/4	7	12.5	ns
STRB_H_LINK	4/4	7	12.5	ns

Figure 9: Clocks (see text for a discussion of allowed clock skew)

Output	Min Clock-to-Output	Max Clock-to-Output	Unit
D_L_OPP	4.8 + 0.024 / pF	8.3 + 0.064 / pF	ns
D_H_OPP	4.7 + 0.024 / pF	8.2 + 0.064 / pF	ns
SOC_L_OPP	5.5 + 0.024 / pF	8.1 + 0.064 / pF	ns
SOC_H_OPP	5.0 + 0.024 / pF	7.7 + 0.064 / pF	ns
DAV_L_OPP	5.7 + 0.024 / pF	8.3 + 0.064 / pF	ns
DAV_H_OPP	4.6 + 0.024 / pF	7.4 + 0.064 / pF	ns
RESET_OPP	3.5 + 0.024 / pF	8.9 + 0.064 / pF	ns

Figure 10: OPP Output Timing

NOTE 1: These signals should be strapped to either logic zero or one at power-up and should not change during normal switch operation. These signals have 10 KOhm pull-up or pull-down resistors on the main switch board.

NOTE 2: These signals are allowed to be asynchronous. Metastability concerns are handled by the IPP. These signals have 10 KOhm pull-up or pull-down resistors on the main switch board.

NOTE 3: Maximum clock frequency (CLK_LINK) is 25 MHz when TCA_LINK is used.

NOTE 4: These numbers were derived from Atmel data book cell and RC delays, after restricting the operating range to 15 to 80 degrees Celsius and 3.3 to 3.45 volts. Refer to [8, Appendix A] for details on the derating factors used to obtain the numbers here.

NOTE 5: Measured Data from Feb. 1998. Measured data does not support the maximum clock-to-output entries in Figure 10. Using what we believe to be typical speed OPP circuits, we measured 9.5 ns clock-to-output on a D_L_OPP line, which we estimate had 15 to 20 pF load. From Figure 10, the maximum clock-to-output delay is (8.3 + 0.064*20) = 9.6 ns with a 20 pF load. Based on Figure 10, we expected to measure a delay value in the 7 to 7.5 ns range. It would thus be prudent for the designer to design for a maximum clock-to-output delay of about 3 ns longer than Figure 10 would indicate. Note the measurements enhance the believability of the minimum clock-to-output numbers. Thus, for the D_L_OPP lines, it is reasonable to design for a clock-to-output delay range (assuming a 20 pF load) of no more than (4.8 + 0.024*20) = 5.3 ns to (9.6 + "about 3") = 12.5 ns. If we allow a receiver (G-link, OC-48, whatever) setup and hold time of 2 ns each, for a total of 4 ns, and we design the clock circuit with no buffering between

Input	Set-Up	Hold	Unit
TCA_FF_LINK	2.4	0.0	ns
TCA_LINK	10.0 (Note 3)	0.0	ns
D_L_LINK	4.4	- 0.5	ns
D_H_LINK	5.2	- 0.3	ns
SOC_L_LINK	4.3	- 1.1	ns
SOC_H_LINK	4.4	- 0.8	ns
UNASSIGN_EN	Note 1	Note 1	
WIDTH_LINK	Note 1	Note 1	
TYPE_LINK[3:0]	Note 1	Note 1	
D_SKEW_LINK	Note 1	Note 1	
PAD_ZERO	Note 1	Note 1	
UP_L_LINK	Note 2	Note 2	
UP_H_LINK	Note 2	Note 2	

Figure 11: OPP and IPP Input Timing

the CLK_LINK signal to the OPP and the clock signal to the receiver, then we have a total of 11.2 ns of time that must fit within one clock period if we assume no hand tuning or matching per OPP - port card pair. An 11.2 ns period is a clock rate of 89 Mhz, which will support an OC-48 connection, but will not support applications that require the ability to assure the OPP buffers do not overflow. These applications require a clock period of 9.5 ns. [(14/16) x (120MHz)] = 105MHz, which is a 9.5 ns period. We expect to have additional data before any OPP buffer draining applications that require the 105 MHz clock reach the detailed timing design stage. There is a good chance that the minimum clock-to-output delay of 5.3 ns can be increased after more data is collected.

5.2 DC Electrical Characteristics: OPP and IPP

The DC electrical characteristics listed in Figure 12 and 13 pertain to the OPP and IPP. These values do not take on-board pull-up/pull-down or termination resistors into account; allowance should be made for both where appropriate.

Parameter	Min	Max	Unit
Voh, Ioh = 3.5mA	2.4	-	V
Vol, Iol = 3.5mA	-	0.4	V

Figure 12: DC Electrical Characteristics of OPP and IPP Outputs

Parameter	Min	Max	Unit
Vil	-0.3	0.8	V
Vih	2.0	VDD5+0.3	V
Iih, Iil (no pull-up/down)	-5.0	+5.0	uA

Figure 13: DC Electrical Characteristics of OPP and IPP Inputs

The IPP and OPP link interface pins use 3.3 Volt output pads and 5 Volt input pads to achieve the minimum clock-to-output delay. VDD5 is the value of the 5 Volt supply at the OPP and IPP.

5.3 Capacitance: OPP and IPP

The capacitance characteristics listed in Figure 14 pertain to the OPP and IPP. These values do not take the Printed Circuit Board (PCB) or connector into account; allowance should be made for both where appropriate.

Parameter	Max	Unit
Cin, Vin = 0V	8	pF

Figure 14: Capacitance

6 Design Examples

6.1 Design Example: 155 Mb/s SONET

The logical design of a 155 Mb/s SONET link interface adapter based on a PMC-Sierra PM5345 SUNI chip [3] is illustrated in Figure 15. Since the FIFOs used by the PM5345 have an asynchronous interface, FSMs are required to

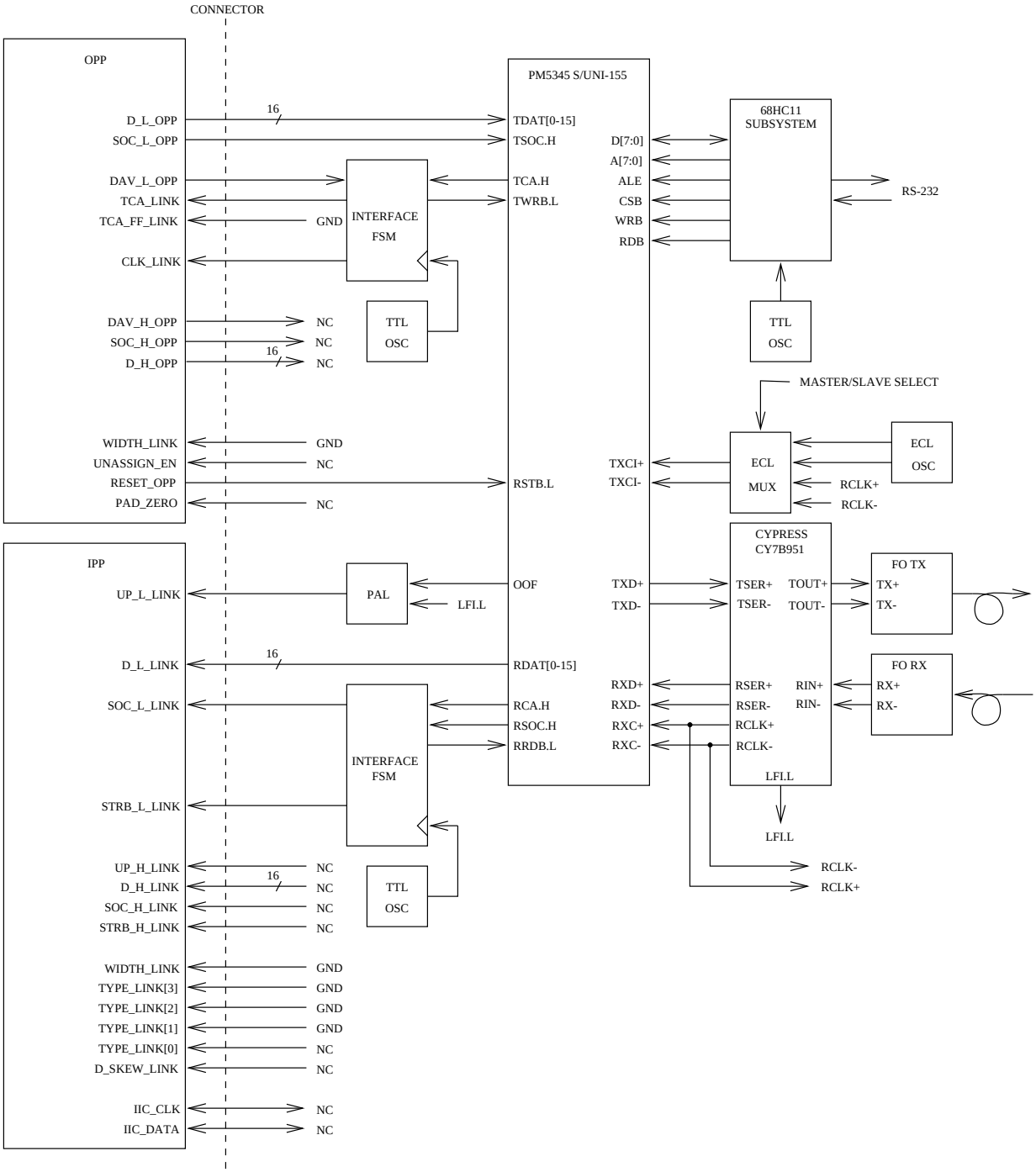


Figure 15: An Example 155 Mb/s SONET Interface

perform the necessary handshakes. This adapter uses the 16-bit mode supported by the OPP and IPP. Cell-level handshaking is implemented by the adapter card using the OPP TCA_LINK signal.

A Motorola M68HC11 microcontroller [10] is used to initialize the PM5345. This microcontroller has on-board EEPROM for program storage. Versions of the microcontroller with on-board monitor programs are also available. When used with the available RS-232C serial link [11] and a terminal, the on-board monitor allows the operation of the PM5345 to be monitored via register access. This capability facilitates debug and line test operations.

This implementation uses a Cypress CY7B951-SC clock recovery module [12] and industry standard, 16-pin Optical Data Links (ODLs). An ECL multiplexer and a 155.52 MHz ECL oscillator are used to provide master/slave capability. When the clock recovered by the CY7B951 is used for transmission, the link adapter operates in slave mode. When the 155.52 MHz local clock is used, the link adapter operates in master mode. In this design, master/slave mode is jumper selectable.

6.2 Design Example: Dual 155 Mb/s SONET

The logical design of a dual 155 Mb/s SONET link interface adapter based on the PMC-Sierra PM5348 S/UNI-Dual chip [4] is illustrated in Figure 16. The PM5348 has on-chip clock recovery circuitry for both channels. Two Hewlett-Packard HFBR-5205 optical data links (ODLs) [7] are used to implement the two fiber interfaces.

The PM5348 registers are programmed using a simple finite-state machine implemented using a PAL. The PM5348 default settings changed via programming are:

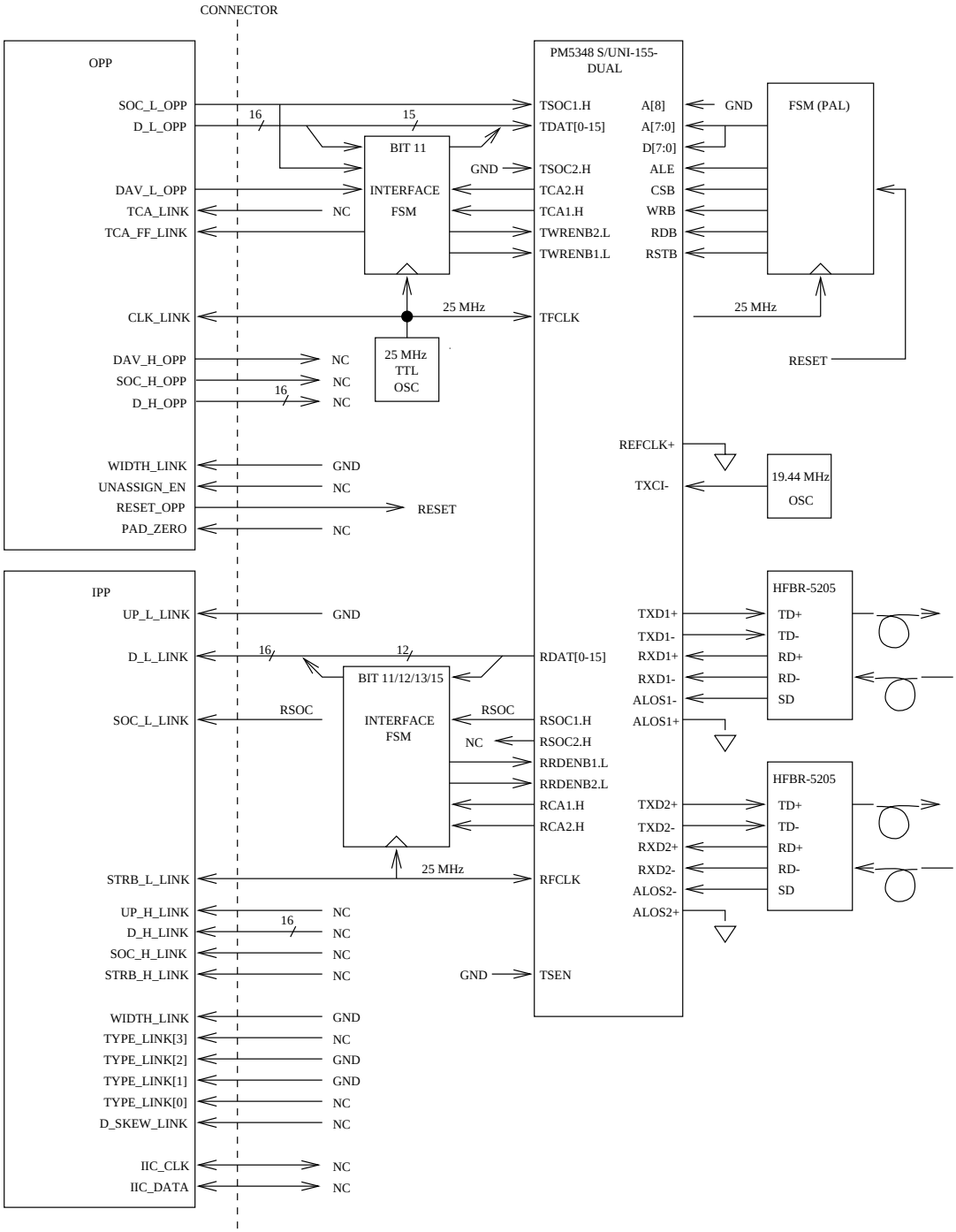


Figure 16: An Example Dual 155 Mb/s SONET Interface

1. The SPLIT bit is set to a logic zero (Register 0x008) to select the multi-PHY interface mode;
2. The BUS8 bit is set to a logic zero (Register 0x008) to select 16-bit bus interface mode;
3. The DISCOR bit is set to a logic 1 (Register 0x050) to disable the error correction algorithm so that any error detected in the cell header is treated as an uncorrectable HCS error;
4. The PASS bit is set to a logic 1 (Register 0x050 and 0x0D0) so that the match header pattern registers are ignored and filtering of cells with VPI and VCI fields set to zero is not performed.

The dual SUNI adapter card has two finite state machines and gating logic between the PM5348 and the connector leading to/from the Gigabit Switch. These finite state machines and gating logic (hereafter referred to as the "glue logic") are designed to allow the Gigabit Switch control software to specify which of the two fibers to use via the most significant bit of the VPI field in the ATM cell header.

The glue logic examines cells from the OPP going to the link interface card. VPI[7], the most significant bit of the VPI (where bit 0 is the least significant bit), selects the fiber on which the cell will be sent by the PM5348 by driving the appropriate control signals of the dual SUNI: TWRENB1.H is driven when VPI[7] is 0, and TWRENB2.H is driven when VPI[7] is 1. Here, we refer to cells as using either fiber 0 (TWRENB1.H) or fiber 1 (TWRENB2.H).

In addition, the VPI[7] bit is always forced to 0 when it is written into the PM5348, regardless of whether it was a 0 or a 1 when it came out of the OPP. This is done because otherwise the range of possible VPIs appearing on fiber 1 is 128 through 255, as opposed to the more desirable 0 through 127. It is better for most ATM equipment to restrict the range of VPIs and VCIs to a range starting at 0. The HEC byte computed and sent out by the OPP is thus incorrect when VPI[7] is changed from a 1 to a 0, but the PM5348 ignores the HEC byte sent to it, and it computes a correct HEC byte over the first four bytes of the ATM cell header. This is the default mode of operation of the PM5348.

The PM5348 has two transmit cell available signals: TCA1.H and TCA2.H. TCA1.H is asserted high if PM5348 is ready to accept a cell for transmission on fiber 0, and TCA2.H is asserted high if the PM5348 is ready to accept a cell for transmission on fiber 1. Since there is only a single transmit cell available signal (TCA_FF_LINK.H) into the OPP, the current design simply asserts TCA_FF_LINK high if and only if both TCA1.H and TCA2.H are asserted. This could lead to "head of line blocking" if the sequence of cells going out of the OPP are not alternating between the two fibers, but without redesigning the OPP, that problem is best solved by having separate buffering for each fiber outside of the OPP. These buffers are not implemented in the current design.

When cells are received from one of the two fibers and sent from the PM5348 to the Gigabit Switch IPP, the fiber on which it was received is identified by the same VPI[7] bit in the header. This "fiber ID" replaces the contents of VPI[7] received from the fiber. Thus, there are really only 128 different VPIs that can be used on each of the two fibers. For the reasons stated above, it is better for this range to be 0 through 127 for both fibers. If the upstream ATM device erroneously sends cells with VPI[7]=1, it would be best to discard them in some manner, and this is done in the current implementation using the method described below.

The method chosen in this implementation for deleting cells received with VPI[7]=1 is to pass what is most likely an incorrect HEC byte to the IPP for such cells, which discards and counts cells with incorrect HECs. Note that when a cell with VPI[7]=0 is received on fiber 1, the glue logic changes VPI[7] to 1 before passing it to the IPP chip. Therefore, since the IPP chip discards cells with incorrect HECs, the glue logic must also correct the HEC. Each bit of the HEC is an exclusive OR of some subset of the other 32 bits of the ATM cell header, possibly inverted. Thus, if the HEC sent out of the PM5348 is correct, changing VPI[7] only requires toggling some subset of the HEC bits in order to correct it. Toggling VPI[7] only requires toggling bits 7, 5, and 4, where bit 0 is the least significant bit of the HEC.

The glue logic implemented in the current design toggles bits 7, 5, and 4 of the HEC if the cell arrived on fiber 1, otherwise it passes the HEC unmodified. This has the behavior summarized in the table below. "Fiber" indicates the number of the fiber on which the cell arrived. "Fiber VPI[7]" is the VPI[7] value in the cell as received on the fiber. "IPP VPI[7]" is the value sent by the glue logic to the IPP, which is always equal to the fiber number. "IPP

HEC" indicates whether the glue logic toggles bits 7, 5, and 4 of the HEC. "IPP HEC correct?" indicates whether the HEC received by the IPP is correct, assuming that it was correct coming out of the PM5348. The end result is that (valid) cells received on the two fibers with VPI[7]=0 are passed correctly, otherwise they are discarded by the IPP because they have (as a result of the operation of the glue logic) an incorrect HEC.

Fiber	Fiber VPI[7]	IPP VPI[7]	IPP HEC	IPP HEC correct?
0	0	0	unmodified	yes
0	1	0	unmodified	no
1	0	1	modified	yes
1	1	1	modified	no

Figure 17: Operational Details of Dual 155 Mb/s SONET Interface "glue logic"

Another alternative that was considered but not implemented was to modify the HEC if and only if the Fiber VPI[7] and IPP VPI[7] were different. This would have the effect that all cells with correct HECs on the fiber would be passed to the IPP with a correct HEC. This would mean that the switch would effectively ignore VPI[7] completely, treating cells received on fiber 0 with VPI=(i+128) exactly as those received on fiber 0 with VPI=i.

6.3 Design Example: 622 Mb/s SONET

The logical design of a 622 Mb/s SONET link interface adapter based on a PMC-Sierra PM5355 SUNI chip is illustrated in Figure 18. This adapter uses the 16-bit mode supported by the OPP and IPP. For transmission, cell-level handshaking is implemented by the adapter card using the OPP TCA_FF_LINK signal. Here, the PM5355 must be programmed to assert TCA four (4) writes before the end of a cell transfer. Handshaking is not performed between the adapter card and the IPP; tying RRDENB.L low supports this mode of operation. Here, the PM5355 supplies cells when they become available without the need for handshaking.

The PM5348 registers are programmed using a simple finite-state machine implemented using a PAL.

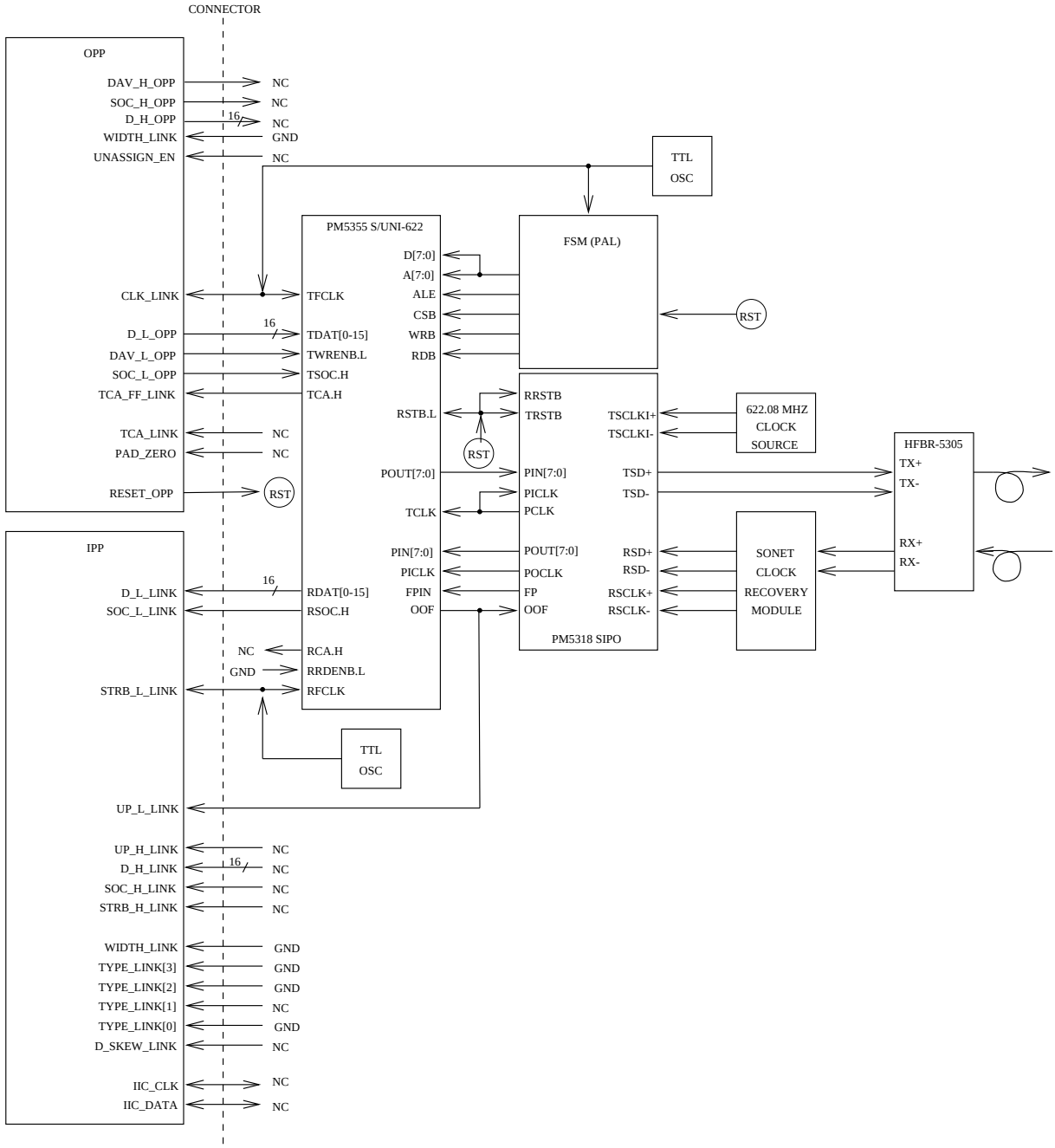


Figure 18: An Example 622 Mb/s SONET Interface

This implementation uses a PMC-Sierra PM5318 Serial-In-Parallel-Out (SIPO) [13] support chip and one of several possible 622.08 MHz clock recovery ICs, e.g., the Vectron Laboratories SCRM-622 [14]. An optical transceiver from Hewlett-Packard [15] is used to implement the optical data link.

If the clock recovered by the SONET clock recovery module is also used for transmission, the link adapter operates in the slave mode. Figure 18 shows the use of a separate 622.08 MHz clock source; use of a separate clock source allows the link adapter to operate as a master. Selectable operation is also possible.

6.4 Design Example: 2.4 Gb/s SONET

The logical design of a 2.4 Gb/s SONET link interface adapter based on SONET transmit and receive subsystems with UTOPIA [2] interfaces is illustrated in Figure 19. This adapter uses the 32-bit mode supported by the OPP and IPP. For transmission, cell-level handshaking is implemented by the adapter card using the OPP TCA_FF_LINK signal. Here, the transmit subsystem must assert TCA four (4) writes before the end of a cell transfer. Handshaking is not performed between the adapter card and the IPP; tying RRDENB.L low supports this mode of operation. Here, the receive subsystem supplies cells when they become available without the need for handshaking.

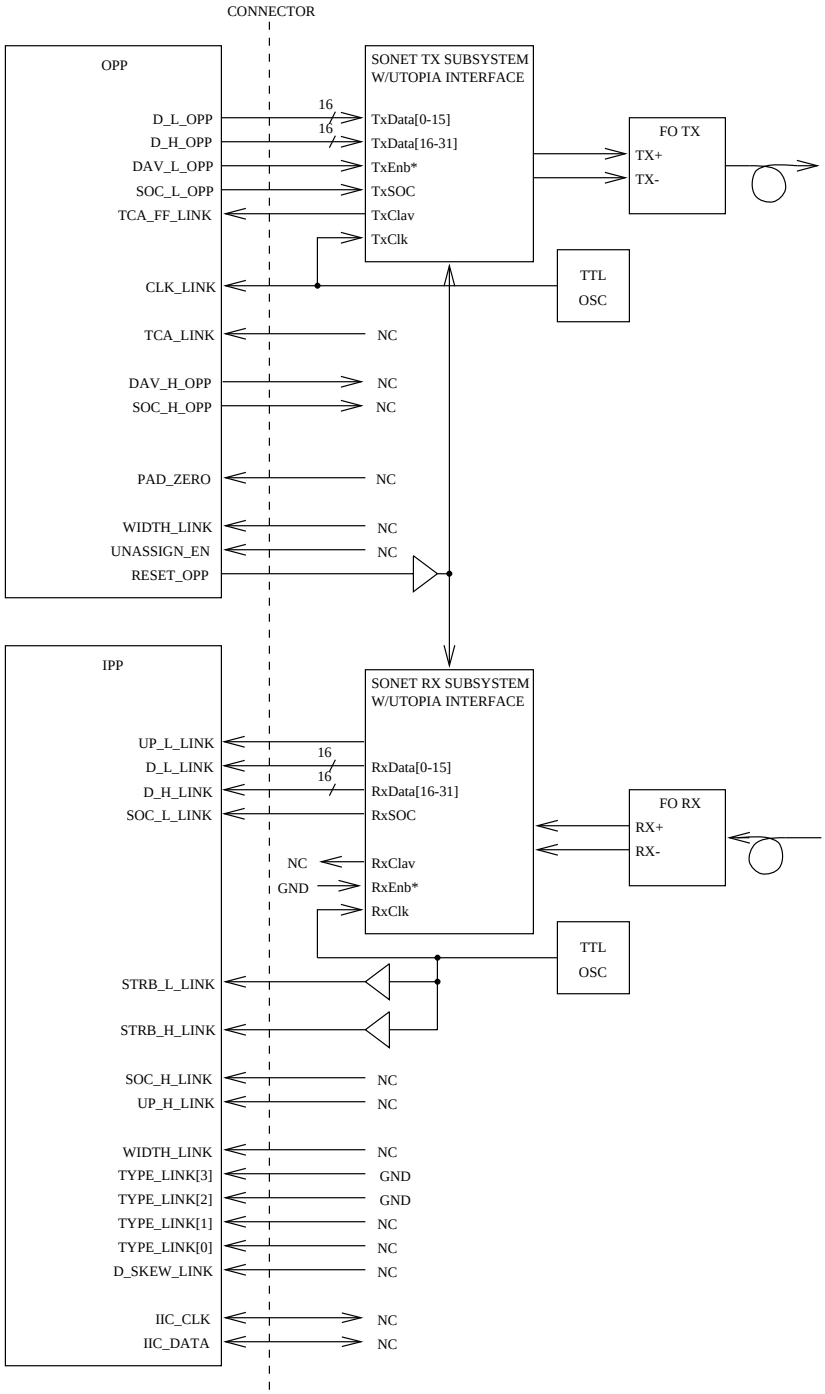


Figure 19: An Example 2.4 Gb/s SONET Interface

This design requires the use of fiber optic transmit and receive devices capable of supporting SONET transmission at 2488.32 Mb/s.

6.5 Design Example: 622 Mb/s / 1.2 Gb/s G-LINK

The logical design of a 622 Mb/s / 1.2 Gb/s G-Link link interface adapter based on an Hewlett-Packard G-Link chip set is illustrated in Figure 20. The data rate is determined by the oscillator shown and option pins on the G-Link chip set. This adapter uses the 16-bit mode supported by the OPP and IPP. For transmission, cell-level handshaking is not required: the G-Link transmitter can accept a 16-bit word for transmission on every clock cycle. Handshaking is not performed between the adapter card and the IPP either: the G-Link receiver supplies cells as a continuous stream of 16-bit words.

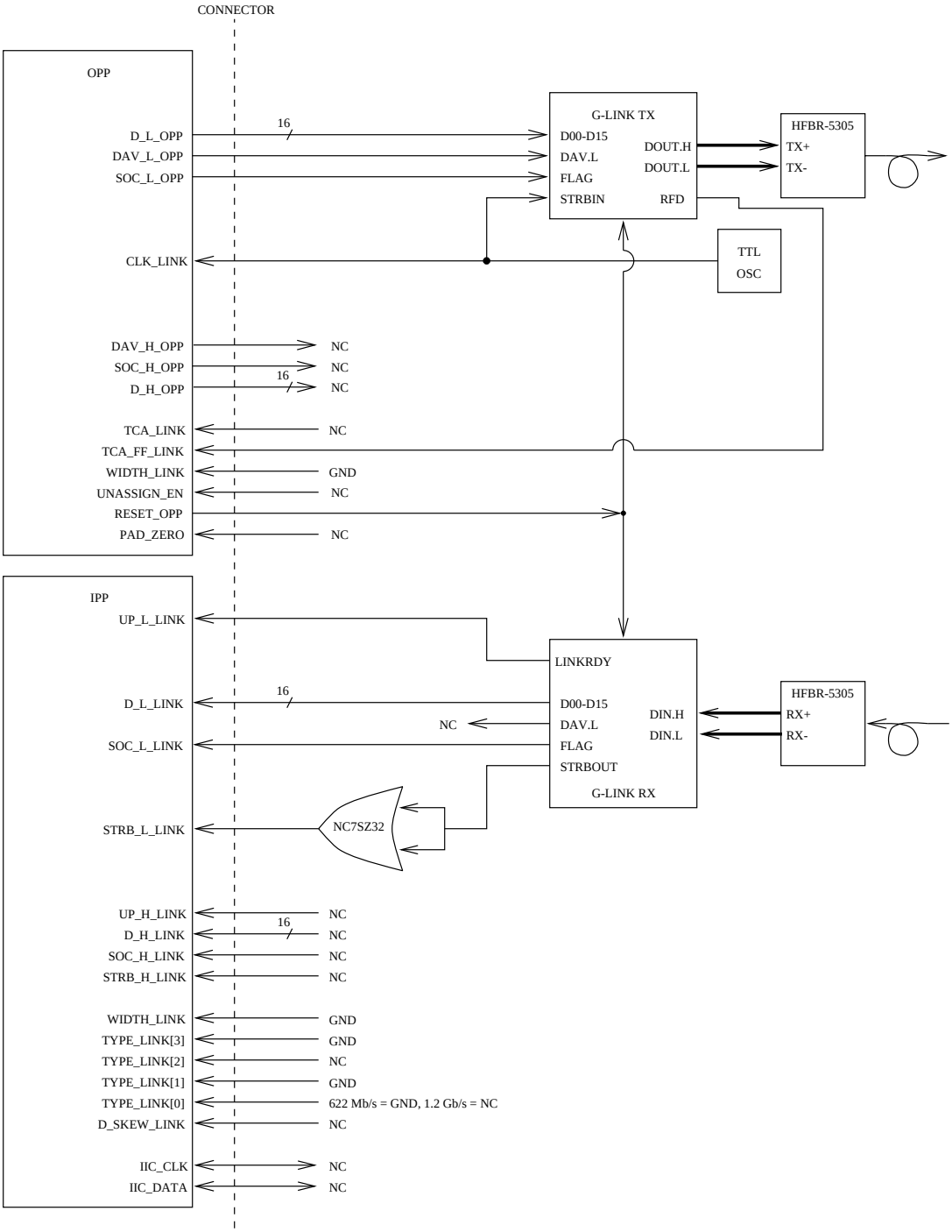


Figure 20: An Example 622 Mb/s / 1.2 Gb/s G-Link Interface

This implementation uses an optical transceiver from Hewlett-Packard [15] to implement the optical data link. Clock recovery is performed by the G-Link receiver.

This design uses the "Ready for Data" (RFD) signal generated by the G-Link transmitter to drive the TCA_FF_LINK OPP input. This signal is asserted when the G-Link transmitter is ready to accept data for transmission.

The LINKRDY signal generated by the G-Link receiver is used to drive the UP IPP input. This signal is asserted low when the start-up sequence is complete and the data and control indications are valid.

6.6 Design Example: 2.4 Gb/s G-LINK

The logical design of a 2.4 Gb/s G-Link link interface adapter based on a pair of Hewlett-Packard G-Link chip sets is illustrated in Figure 21. The data rate is determined by the oscillator shown and option pins on the G-Link chip sets. This adapter uses the 32-bit mode supported by the OPP and IPP in conjunction with the de-skewing circuitry implemented in the IPP. For transmission, cell-level handshaking is not required: the G-Link transmitters can each accept a 16-bit word for transmission on every clock cycle. Handshaking is not performed between the adapter card and the IPP either: the G-Link receivers supply cells as a continuous stream of 16-bit words.

Unassigned cells are transmitted to the adapter card by the OPP when a valid cell is not available for transmission. These cells are delivered by the G-Link transmission subsystem to the IPP. The de-skewing circuitry inside the IPP uses these cells to compensate for clock skew.

This implementation uses a optical transceivers from Hewlett-Packard [15] to implement the optical data link. Clock recovery is performed by the G-Link receivers.

This design uses the logical AND of the "Ready for Data" (RFD) signals generated by the G-Link transmitter to drive the TCA_FF_LINK OPP input. These signals are asserted when the G-Link transmitters are ready to accept data for transmission.

The LINKRDY signals generated by the G-Link receivers are used to drive the UP IPP inputs. These signal are asserted low when the start-up sequence is complete and the data and control indications are valid.

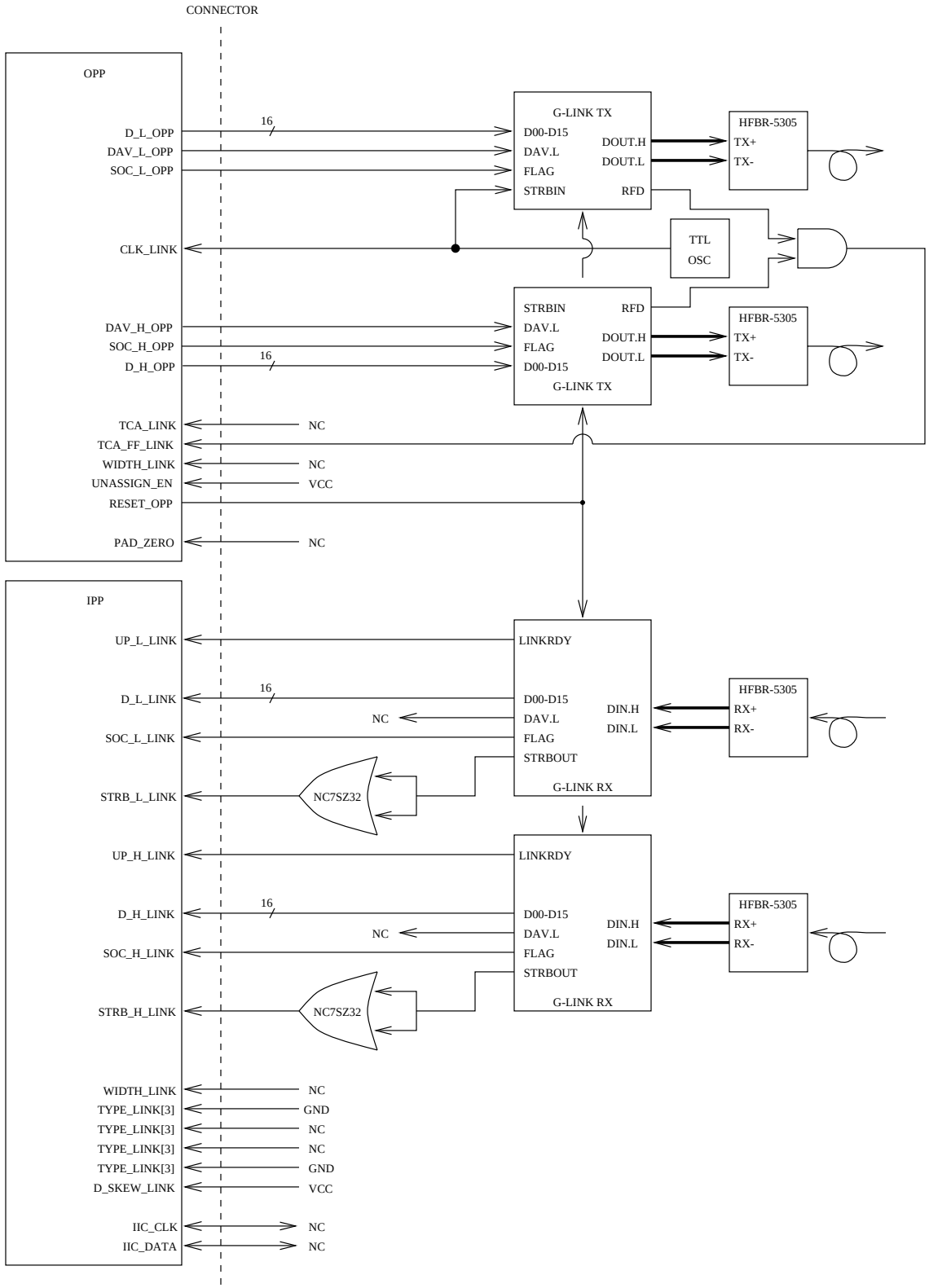


Figure 21: An Example 2.4 Gb/s G-Link Interface

7 Physical Adapter Card Specifications

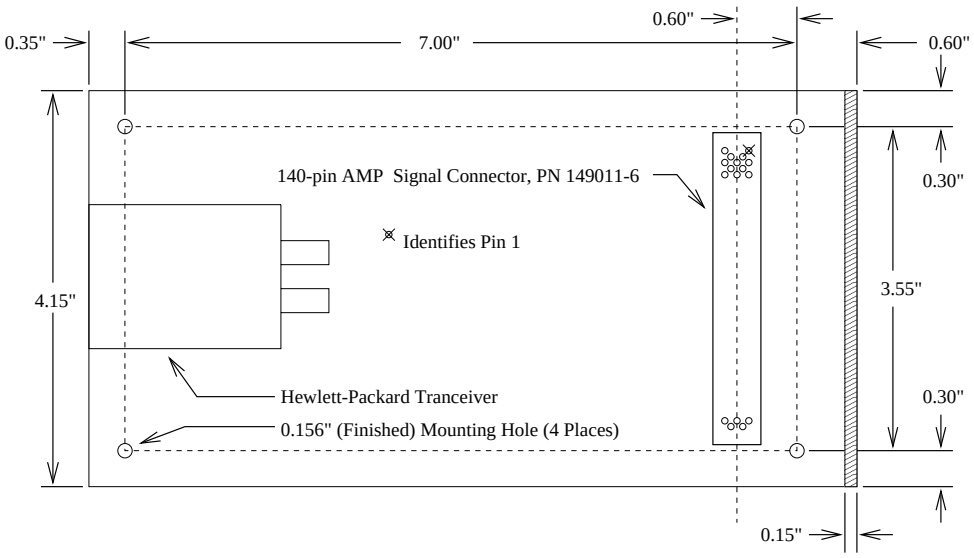
Adapter cards are required to be 4.15 inches by 7.90 inches in size with the connector located as shown in the scaled drawing of Figure 22. The adapter card connector is a 140-pin AMP connector (AMP part number 149011-6); the mating connector is used on the main switch board (AMP part number 536255-6). Figure 22 shows the view from the top, or component, side of the adapter card. The physical connector is located on the bottom, or solder, side of the adapter card. A detail of the physical connector pin assignment is shown in Figure 23. This view is from the solder-pin-side of the connector.

Power is supplied to each link interface adapter via pins on the 140-pin AMP connector, and +5.0 V, +3.3 V, and -5.2 V supplies are available. The power supply in the prototype switch is capable of supplying up to the maximum current listed in Figure 24 on each of the +5.0 V, +3.3 V, and -5.2 V connections to each adapter card.

Supply	Current
+5.0 V	3.0 A maximum, +4.95 V to +5.25 V
+3.3 V	0.75 A maximum, +3.30 V to +3.60 V
-5.2 V	0.3 A maximum, -5.05 V to -5.45 V

Figure 24: Power Supply Ratings

If additional current and/or voltages are required, the Washington University design team should be consulted. (For example, the above listed maximum currents supplied to six of the eight adapter card slots allows the last two adapter card slots to draw up to 5 A at +5 V, up to 2 A at +3.3 V, and up to 2.5 A at -5.2 V.)



Note: Cross-hatched area must be free of components, both sides of board.

Note: The central 3.75" by 6.40" area of the adapter card can have parts on the solder (bottom) side fo the board up to 0.625" high. All of the component side of the board (top) can have components up to 0.625" high.

Figure 22: Scale drawing of a link interface adapter card; view from the component side of the adapter card, solder side of the connector.

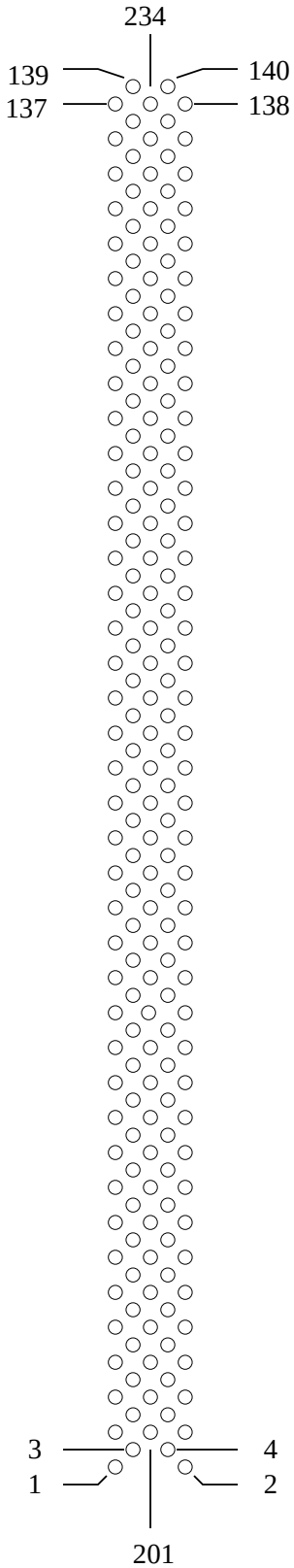


Figure 23: 200-pin connector pin assignment; view from the component side of the adapter card, solder side of the connector.

The recommended physical placement of the transceiver on an adapter card is shown in Figure 22. Transceivers should be located so that the fiber pair can make a 90 degree bend while above the associated link adapter card; this will allow fibers to be routed to the front wiring panel without interfering with neighboring adapter cards.

7.1 Prototype Switch Chassis Air Flow Specification

The prototype Washington University Gigabit Switch (WUGS-20) is designed to operate in a laboratory environment. The inlet air temperature, therefore, can be expected to remain between 15 and 35 degrees C. The area reserved for the eight link interface adapters will have a forced air flow rate of approximately 1.5 m/s. Air flow across each of the eight link adapters in a prototype switch will be perpendicular to the long axis of the link adapter, and the link adapter nearer the air outlet will be cooled by air that has passed over the link adapters nearer the air inlet. The change in temperature of the air flowing across the link interface adapters nearer the air inlet is expected to be only a few degrees C.

Interface designs that have cooling requirements that tax the air temperature and air flow rates specified here should be completed in concert with the Washington University Gigabit Switch design team.

7.2 Interface Connector Pin Assignment

Signal Name	Pin
DAV_L_OPP	4
SOC_L_OPP	3
D_L_OPP<0>	8
D_L_OPP<1>	7
D_L_OPP<2>	10
D_L_OPP<3>	9
D_L_OPP<4>	14
D_L_OPP<5>	13
D_L_OPP<6>	16
D_L_OPP<7>	15
D_L_OPP<8>	20
D_L_OPP<9>	19
D_L_OPP<10>	22
D_L_OPP<11>	21
D_L_OPP<12>	26
D_L_OPP<13>	25
D_L_OPP<14>	28
D_L_OPP<15>	27
CLK_LINK	31
DAV_H_OPP	32
SOC_H_OPP	35
PAD_ZERO	36
D_H_OPP<16>	40
D_H_OPP<17>	39
D_H_OPP<18>	42
D_H_OPP<19>	41
D_H_OPP<20>	45
D_H_OPP<21>	46
D_H_OPP<22>	47
D_H_OPP<23>	48
D_H_OPP<24>	52
D_H_OPP<25>	51
D_H_OPP<26>	54
D_H_OPP<27>	53

D_H_OPP<28>	58
D_H_OPP<29>	57
D_H_OPP<30>	60
D_H_OPP<31>	59
TCA_LINK	63
TCA_FF_LINK	64
UNASSIGN_EN	67
RESET_OPP	68
WIDTH_LINK	71
D_SKEW_LINK	72
TYPE_LINK<0>	73
TYPE_LINK<1>	74
TYPE_LINK<2>	77
TYPE_LINK<3>	78
UP_L_LINK	79
UP_H_LINK	80
D_L_LINK<0>	84
D_L_LINK<1>	83
D_L_LINK<2>	86
D_L_LINK<3>	85
D_L_LINK<4>	90
D_L_LINK<5>	89
D_L_LINK<6>	92
D_L_LINK<7>	91
D_L_LINK<8>	96
D_L_LINK<9>	95
D_L_LINK<10>	98
D_L_LINK<11>	97
D_L_LINK<12>	101
D_L_LINK<13>	102
D_L_LINK<14>	103
D_L_LINK<15>	104
SOC_L_LINK	107
STRB_L_LINK	108
D_H_LINK<16>	112
D_H_LINK<17>	111
D_H_LINK<18>	114
D_H_LINK<19>	113
D_H_LINK<20>	118
D_H_LINK<21>	117
D_H_LINK<22>	120
D_H_LINK<23>	119
D_H_LINK<24>	124
D_H_LINK<25>	123
D_H_LINK<26>	126
D_H_LINK<27>	125
D_H_LINK<28>	130
D_H_LINK<29>	129
D_H_LINK<30>	132
D_H_LINK<31>	131
SOC_H_LINK	135
STRB_H_LINK	136
IIC_DATA	139
IIC_CLK	140

GND	201,202,203,204,205,206,207,208,209,210
GND	211,212,213,214,215,216,217,218,219,220
GND	221,222,223,224,225,226,227,228,229,230
GND	231,232,233,234
GND	87,88,93,94,99,100,105,106,109,110,115,116
GND	121,122,127,128,133,134,137,138
NC	69,75,76
+5v	1,2,5,6,11,12,17,18,23,24
-5.2v	29,30,33,34,37,38,43,44,49,50
+3.3v	55,56,61,62,65,66,70,81,82

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[2] "UTOPIA, an ATM-PHY Interface Specification," Level 1, Version 2.01, The ATM Forum, March 21, 1994.

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