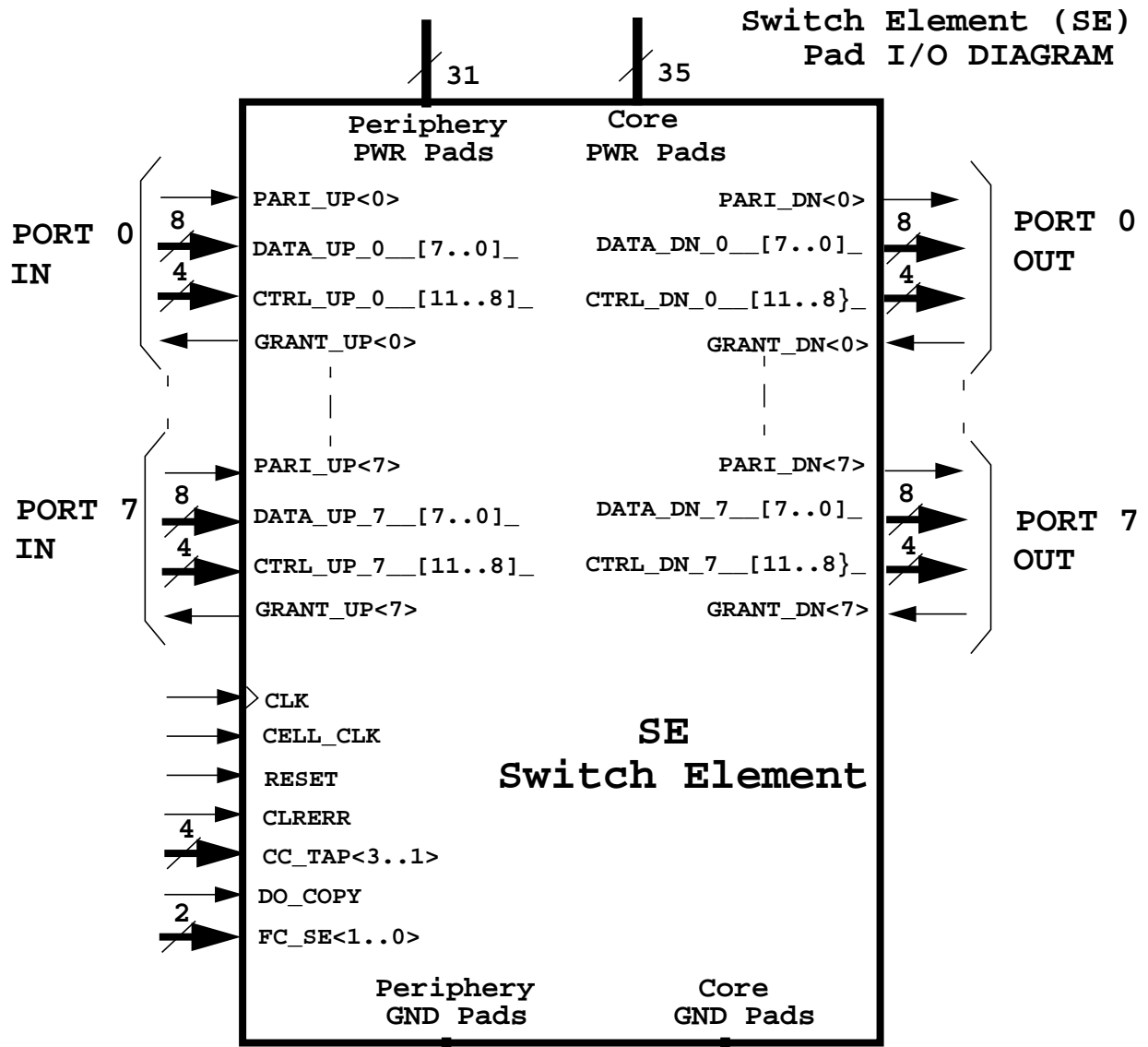


Working Note ARL-96-05**SE Signal Description****June 23, 1998 (Version 1.0)****by:****Thomas J. Chaney****Fred U. Rosenberger**

This document provides the Input and Output signal description, position, and timing for the Switch Element (SE) integrated circuit used in the Washington University Gigabit Switch described in "System Architecture Document for GIGABIT SWITCHING TECHNOLOGY," Version 3.1, Working Note ARL-94-11, by Jonathan S. Turner and staff.



| Chip Pads | Package Pins |
|-------------------------|-----------------|
| INPUT : 123 | 123 |
| OUTPUT: 112 | 112 |
| Power : 66 | 21 |
| Ground: 58 | 22 |
| Unused: - | 21 |
| Total : 359 Pads | 299 Pins |

Figure 1
Switch Element (SE) chip I/O Diagram

Signal Descriptions:

DATA_UP [**port number**][**bit number**]_ (Input) Each of the eight input ports receives eight bits of data each clock period. The ports are labeled 0 through 7, and the eight bits of data to each port are labeled 0 through 7.

CTRL_UP [**port number**][**bit number**]_ (Input) Each of the eight input ports receives four bits of control each clock period. The ports are labeled 0 through 7, and the four control bits are labeled 8 through 11. For some purposes, it is best to think of the DATA and CTRL being a twelve bit data group. Thus the control bits are labeled 8 through 11 rather than 0 through 3.

PARI_UP<**port number**> (Input) Each of the eight ports receives a parity bit each clock period. Parity is odd (the number ONEs in the 13 signals including the parity bit is odd).

GRANT_UP<**port number**> (Output) Each of the eight ports transmits a grant type handshake signal that indicates whether the port can receive another cell during the next cell period. A new grant signal is transmitted once each cell clock period. (Once every sixteen clock periods.)

DATA_DN [**port number**][**bit number**]_ (Output) Each of the eight output ports transmits eight bits of data each clock period. The ports are labeled 0 through 7, and the eight bits of data from each port are labeled 0 through 7.

CTRL_DN [**port number**][**bit number**]_ (Output) Each of the eight output ports transmits four bits of control each clock period. The ports are labeled 0 through 7, and the four bits of control are labeled 8 through 11. For some purposes, it is best to think of the DATA and CTRL being a twelve bit data group. Thus the control bits are labeled 8 through 11 rather than 0 through 3.

PARI_DN<**port number**> (Output) Each of the eight ports transmits a parity bit each clock period. Parity is odd (the number ONEs in the 13 signals including the parity bit is odd). Parity, once transmitted as incorrect parity, will continue to be transmitted as incorrect parity until the "CLRERR" signal is asserted.

GRANT_DN<**port number**> (Input) Each of the eight ports receives a grant type handshake signal that indicates whether the port can transmit another cell during the next cell period. A new grant signal is received once each cell clock period. (Once every sixteen clock periods.)

CLK (Input) Input clock to SE chip.

CELL_CLK (Input) The SE chip receives a cell clock signal that has a period sixteen times that of the CLK signal. (The form of the CELL_CLK signal is one clock period high, fifteen clock periods low.) The CELL_CLK, RESET, and CLRERR signals are the only signals that must meet a setup and hold relationship with the CLK signal.

RESET (Input) (Asserted Low) The SE chip receives a reset signal that must meet a setup and hold time relationship with the CLK transition two CLK cycles before the clock transition for which CELL_CLK is high. Circuit simulations have shown that asserting the reset signal for 160 clock periods (or more) is adequate for proper circuit operation.

CLRERR (Input) (Asserted Low) The CLRERR signal has the same setup and hold time relationship with the CLK signal as the RESET signal. The CLRERR (clear error) signal resets the parity error. Circuit simulations have shown that asserting the CLRERR signal for 160 clock periods (or more) is adequate for proper circuit operation.

CC_TAP<bit number>¹ (Input) These signals were included to compensate for an expected non-integer cell propagation time through the SE. Since the cell propagation time is an integer cell time (16 CLK periods) with the present SE design, CC_TAP is set to zero in the present switch. The timing relationship between the CELL_CLK and the incoming cell data is set with this four bit field. Circuit simulations have shown that setting these four bits 160 clock periods (or more) prior to the end of the RESET period is adequate for proper circuit operation. The four signals are typically connected to physical switches or jumpers. CC_TAP = 0000 (binary) sets the timing relationship between the incoming cell and the CELL_CLK such that the first word of a cell is expected at the input to the SE chip shortly after the clock period for which the CELL_CLK is positive. (See the timing diagrams in Figure 3 for a more detailed timing relationship between the data and the CELL_CLK.) CC_TAP = 0001 (binary) sets the timing relationship such that the first word of a cell is expected one CLK period later, etc.

DO_COPY (Input) Sets the last rank of switch elements to do a “copy to the same port” operation. Circuit simulations have shown that setting this signal 160 clock periods (or more) prior to the end of the RESET period is adequate for proper circuit operation.

FC_SE<bit number> (Input) This two bit field sets the function of the SE chip to that of a distribution element, a route and copy element, or one to the two possible mixed [distribution - route and copy] networks. Circuit simulations have shown that setting this signal 160 clock periods prior to the end of the RESET period is adequate for proper circuit operation.

Core PWR These pads supply 3.3V to the core (logic circuits) of the chip. This is distinct (and electrically isolated in the chip) from the periphery (pad drivers/receivers) power.

Periphery PWR These pads supply 3.3V to the periphery (pad drivers/receivers) of the chip. This is distinct (and electrically isolated in the chip) from the core (logic circuits) power. Core and periphery power are connected on the package power plane. Package power pins connect to both core and periphery power.

Core GND These pads supply ground to the core (logic circuits) of the chip. This is distinct (and electrically isolated in the chip) from the periphery (pad drivers/receivers) ground.

Periphery GND These pads supply ground to the periphery (pad drivers/receivers) of the chip. This is distinct (and electrically isolated in the chip) from the core (logic circuits) ground. Core and periphery ground are connected on the package ground plane. Package ground pins connect to both core and periphery ground.

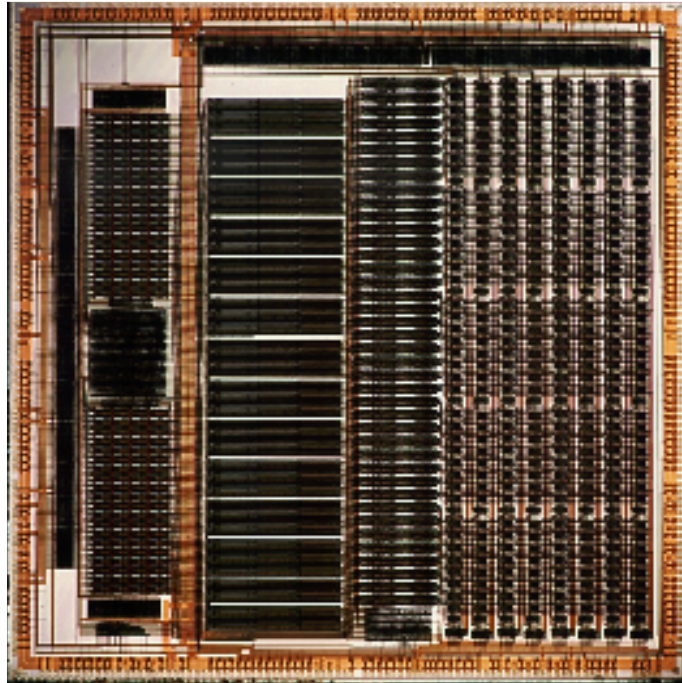
1. These signals were included to compensate for an expected non-integer cell propagation time through the SE. Since the cell propagation time is an integer cell time (16 CLK periods) with the present SE design, CC_TAP is set to zero in the present switch.

Chip Physical Specifications:

The signal names used in Figure 1 are the same signal names used in the SE_TOP.pin file that is generated as part of the design flow for each circuit. The SE_TOP.pin file for the Switch Element chip is attached as Appendix A. The SE_TOP.pin file lists the chip SIGNAL pads in the order they appear around the edge of the chip. The power and ground pads are then listed. The "PAD CENTRE COORDINATES" column must be used to determine the interleaving of power and ground pads with the signal pads. The "BND PIN" column of the SE_TOP.pin file lists the package cavity bonding land number. The SIGNAL bonding land numbers, numbers 1 through 256, map to the ES2 299 pin PGA package pin designations, "A1" through "X20" (See Appendix B). The 299 PGA package used to house the SE chip has power and ground planes within the package. Thus the power and ground PINS on the PGA package do not map directly to the power and ground PADS on the chip. As detailed in Appendix B, there are a total of 21 power and 22 ground pins on the package. (Note, from Figure 1, that there are a total of 66 power and 58 ground PADS on the chip.) The SE chip layout, Figure 2, indicates the coordinates on the chip which are used with the Table of Appendix A to identify the position of each pad.

7225, 7095

7225, -7095



-7225, 7095

-7225, -7095

Figure 2
Switch Element Chip with Coordinate
system used in Appendix A shown.

SIGNAL TIMING:

The general timing values and conditions for all three GigaBit Switch chips (SE, IPP, and OPP) are given in ARL-96-04. Information specific to the Switch Element is given here.

INPUT SIGNAL TIMING

The SE chip input circuits include clock-to-data deskewing circuits which adjust the timing of the data path, relative to the clock, over approximately two clock periods. These circuits significantly increases traditional signal-timing tolerances.

CLK: up to 88MHz, 40%-60% worst case duty factor, rise and fall times < 2ns. (Design goal of 120MHz, worst case, was not met with the first version of the SE chip.)

CELL_CLK: setup time = 1.75ns, hold time = 1.00ns

RESET, CLRERR: clocked on the positive clock transition two transitions before the transition for which the CELL_CLK signal is high. Detailed timing is shown in Figure 4.

GRANT_DN: The general timing of GRANT_DN, relative to CELL_CLK and the value of CC_TAP, is shown in Figure 3. GRANT_DN is sampled once per CELL_CLK period on the (8+ <CC_TAP value>)th clock transition following the transition for which the CELL_CLK signal is high.

Data signal groups: There are three groups of signals, each with their own deskewing circuit. The general timing, including the relationship between the ATM cell word position relative to CELL_CLK based on the value of CC_TAP, is shown in Figure 3. Groups 1, 2, and 3 must satisfy the skew requirements as outlined in Working Note ARL-96-04:

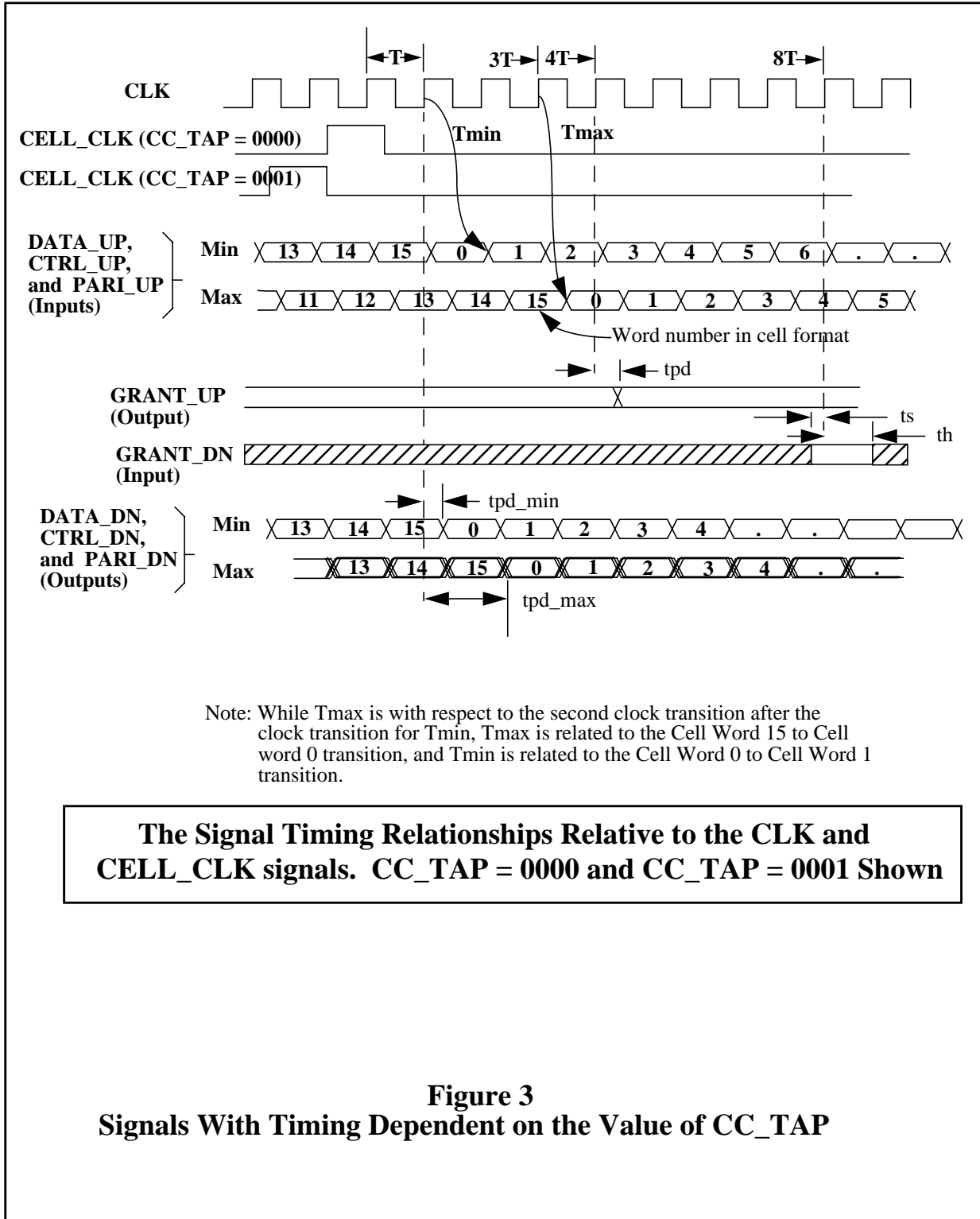
Group 1 (5 bits): Group Control Signal: DATA_UP_x_0_
Other signals: DATA_UP_x_1_ to DATA_UP_x_4_

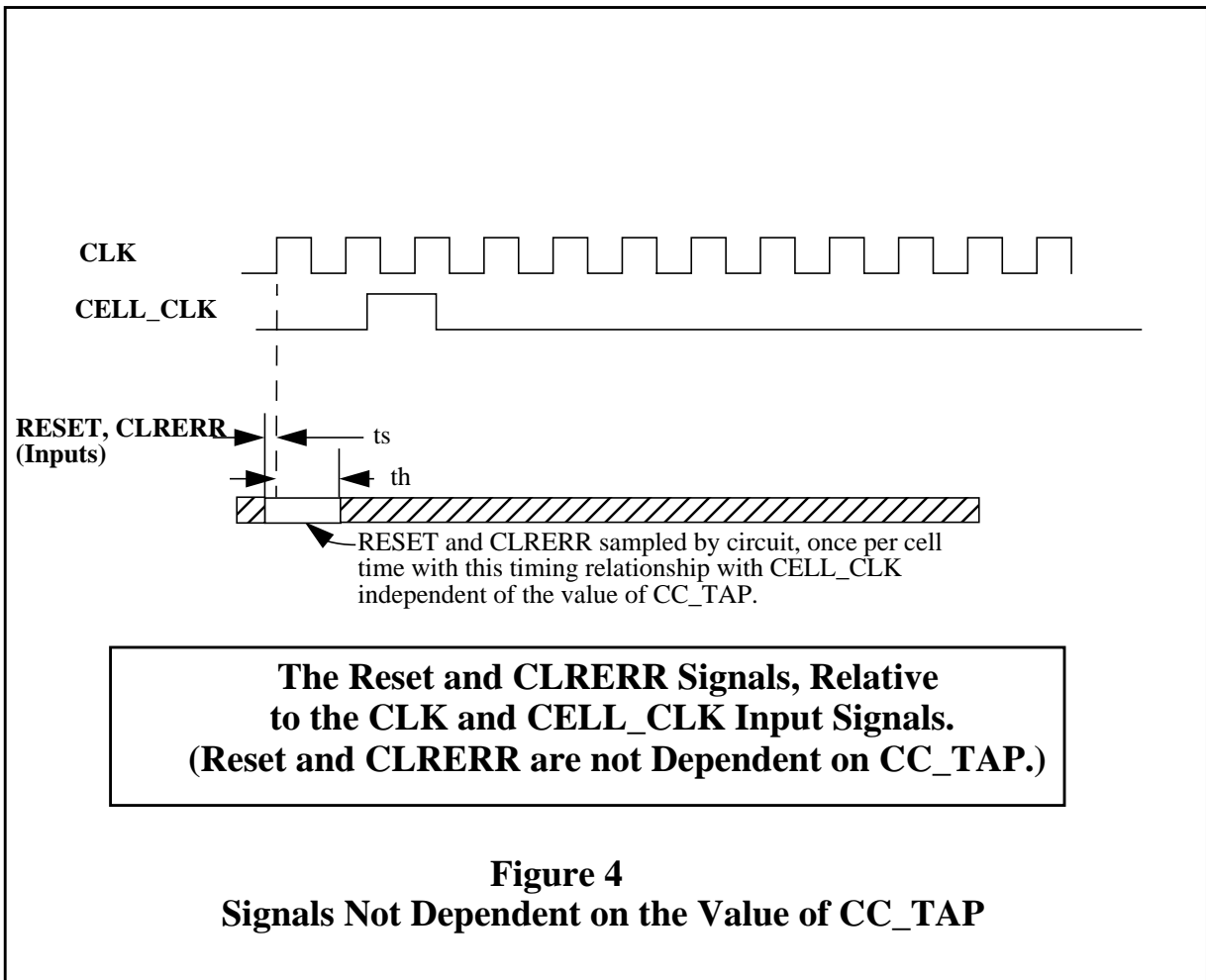
Group 2, (4 bits): Group Control Signal: DATA_UP_x_5_
Other signals: DATA_UP_x_6_, DATA_UP_x_7_, CTRL_UP_x_8_

Group 3, (4 bits): Group Control Signal: CTRL_UP_x_9_
Other signals: CTRL_UP_x_10_, CTRL_UP_x_11_, PARI_UP<x>

OUTPUT SIGNAL TIMING

With the exception of the GRANT_UP signal, all outputs may change each clock period. The GRANT_UP signals may change once per CELL_CLK period, on the (4 + <CC_TAP value>)th clock transition following the transition for which the CELL_CLK signal is high. Detailed timing is shown in Figure 3.





Appendix A

(Print out of the pin_package_rpt_APPENDIX_A.txt file, this directory)
(pages A-1 through A-10)

Appendix B

(Copy of 299 PGA pinout from data book)
(Page 35 of Atmel/ES2 Package Selector Guide, Rev. AG4-AO02/J, Oct. 1994)

Appendix C

(Copy of Bonding Diagrams Submitted to Atmel/ES2)
(4 pages)

The package used for the SE chip is a 299 pin PGA package with an internal power and ground plane. The use of the power and ground planes in the package force a fixed package pin assignment for the package power and ground outside pins. Inside the bond cavity, the power and the ground planes each appear as fixed location bond land *regions* around the bond cavity. These bonding regions vary in size from an area large enough to support bonds to seven power or ground chip pads, to an area the same size as the signal bonding lands. Also, the placement of a power or ground pad around any part of the periphery of the chip that is not lined up with the appropriate power or ground region can not be effectively fed from the package. The inductance of a signal pin circuit is so much higher than the inductance of a power or ground plane connection circuit that there is little value in making a power or ground connection using a signal pin circuit. However, to effectively feed the core circuit from the pad ring power, it is often helpful to place a power or ground pad in the pad ring and use this pad to only feed power to the core. Thus chip designs end up with power and ground pads that are not intended to be bonded. The Atmel/ES2 software tool set does not support this package very well. Thus there is some hand drawn work required to complete the bonding diagrams. To assure there are no errors in the hand drawn work, there are four pages of bonding diagrams.

The four pages of bonding diagrams are attached as this Appendix C. The first page details the extent of the hand work, and points out the core power feed pads on the chip that do not receive bond wires. The second page shows all the bonds on one diagram. Page two is a repeat of page one without all the notes. The package cavity is a two tier design. The bond connections to just the bottom(inside) tier is shown on the third page, and the bonds to just the top (outer) tier is shown on page four.