# Working Note ARL-96-06

# IPP Signal Description

## January, 2 1997 (Version 0.2)

## November 7, 1997 (Version 0.3)

**by:**

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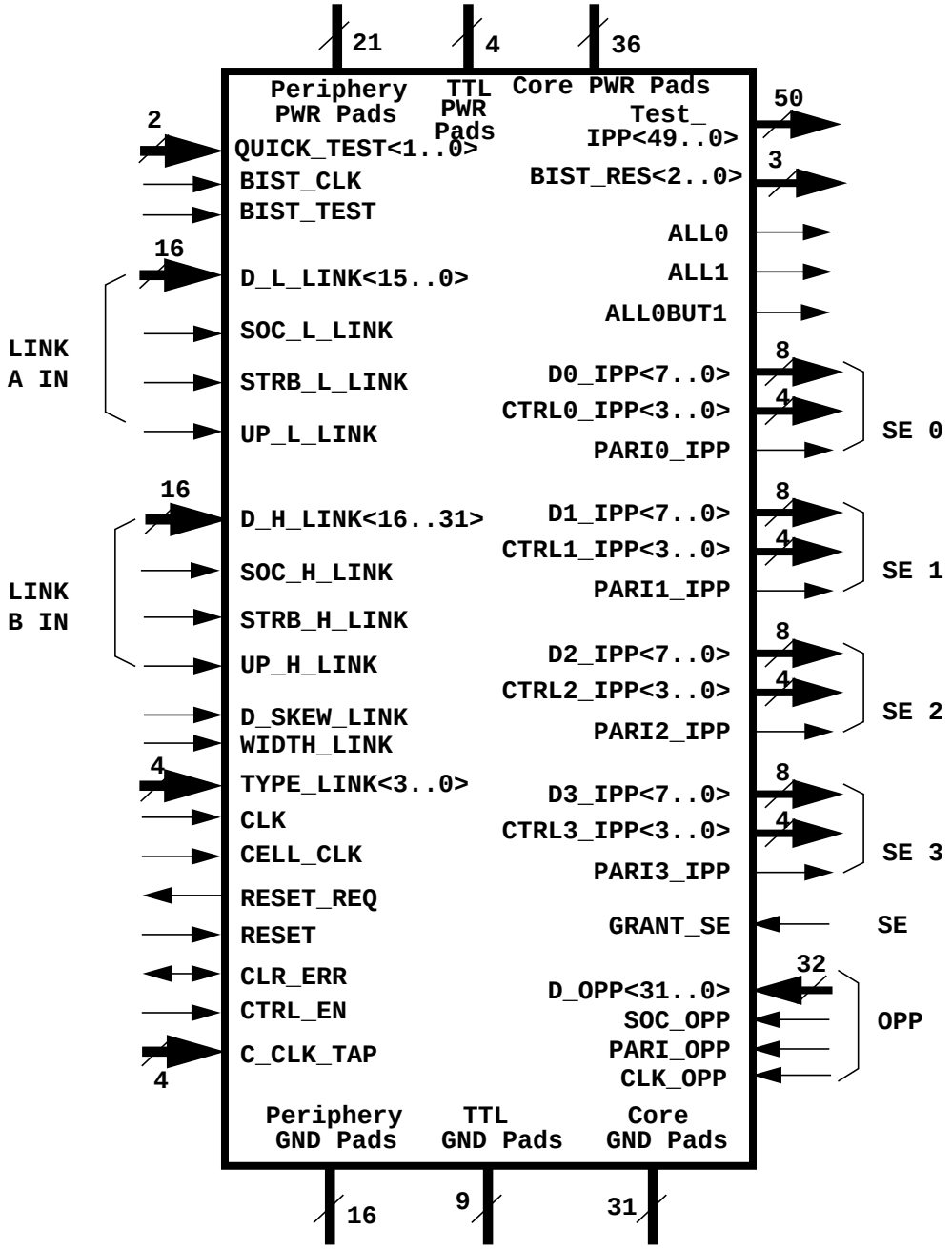
This document gives the Input and Output signal description, position, and timing for the Input Port Processor (IPP) integrated circuit used in the Washington University Gigabit Switch described in "System Architecture Document for GIGABIT SWITCHING TECHNOLOGY, Version 3.1, Working Note ARL-94-11, by Jonathan S. Turner and staff.

Major changes from version 0.1:

- Added a signal between the IPP and the OPP (CLK_OPP).
- Added test pins and descriptions.
- Modified number and location of power and ground pads.
- Changed min. setup from 4.5 to 5.3ns on the link interface. (See **Link Interface Signals** section and ARL-94-17)
- Added setup and hold timing details to **GENERAL INPUT SIGNAL TIMING** section.

## INPUT PORT PROCESSOR(IPP) I/O DIAGRAM




INPUT : 92 pads
OUTPUT:109 pads
IN/OUT: 1 pads
3.3V Power : 57 pads
5.0V Power : 4 pads
3.3V & 5.0V Grounds: 56 pads

Total: 319 pads

**Figure 1**
**Input Port Processor (IPP) chip I/O Diagram**

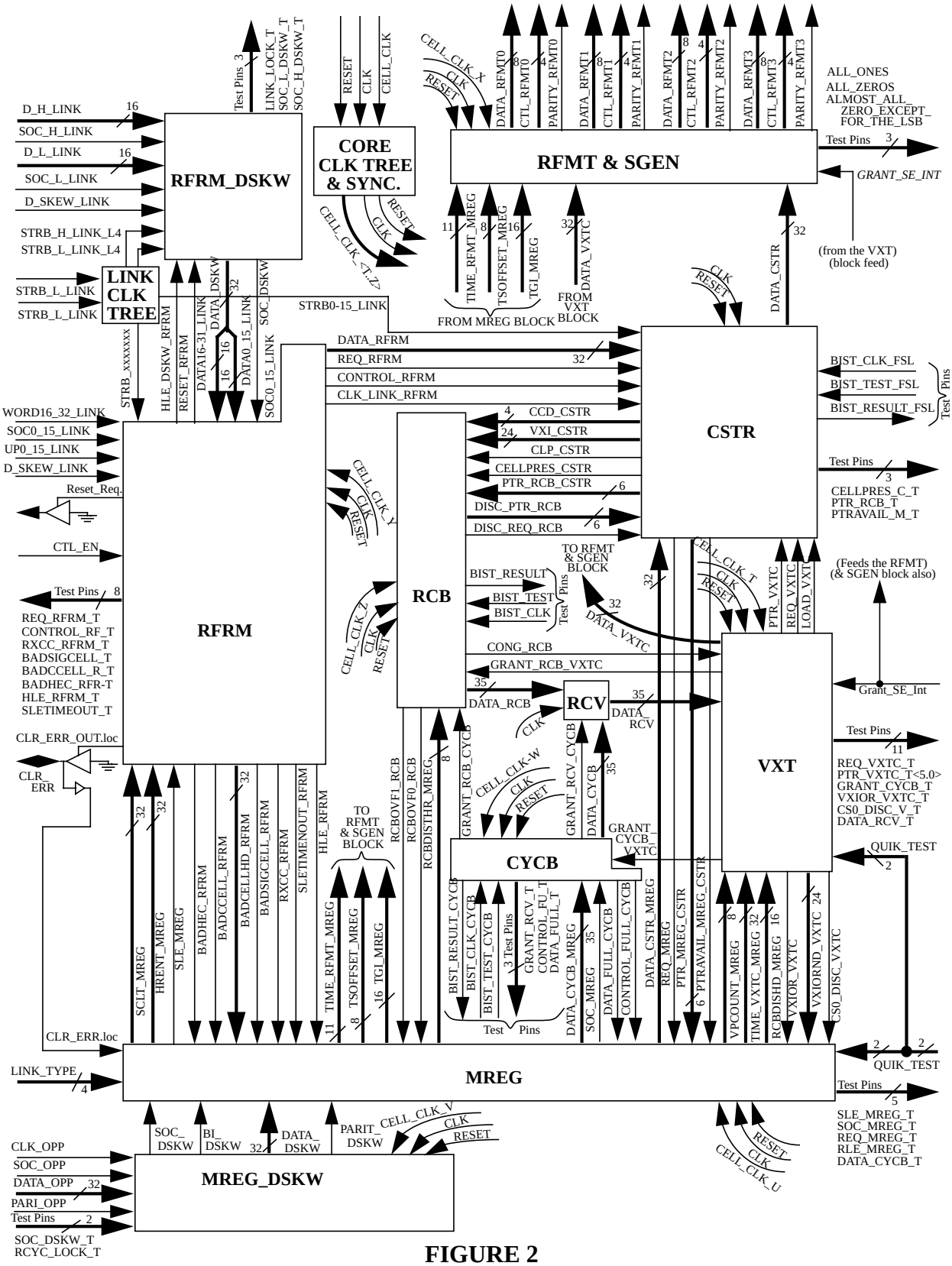



**FIGURE 2**

IPP Detailed Block-to-Block Signaling

## Signal Descriptions:

The IPP provides an interface between the ATM port "link" with its associated clocking, and the switch core with its associated core clock. The signaling within the switch core utilizes a clock-to-data deskewing circuit and a high (120mhz) clock rate. The I/O signaling, described in this document, is shown in Figure 1. Figure 2 shows the I/O signaling along with the signaling between the major logic blocks that make up the IPP. The reader may find it useful to reference Figure 2 during the test pin descriptions. The signaling associated with the ATM link interface is described in great detail in "The Gigabit Switch Link Interface Specification" by W. D. Richard, Version 4.1, Working Note ARL-94-17, Jan. 18, 1996. The ATM link signals will only be listed in this document. The signals associated with the switch core, and the test signals associated with the IPP will be described in this document.

## Link Interface Signals: (Described in W. D. Richard)

**WIDTH_LINK** (Input) A static level, sets the link data interface to 16 or 32 bit data word.

**TYPE_LINK<3 . . 0>** (Inputs) Static levels, sets bit rate and data format (SONET, or G-Link)

**STRB_L_LINK** (Input) The link "clock" for the lower 16 data bits and the "L" SOC signal.

**STRB_H_LINK** (Input) The link "clock" for the upper 16 data bits and the "H" SOC signal.

**D_SKEW_LINK** (Input) Enables the upper 16 bit deskewing circuit for "Dual G-Link" mode.

**D_L_LINK <15 . . 0>** (Inputs) The link lower 16 data bits.(**Version 0.2:** ***The SETUP time has changed from 4.5 to 5.3ns min. The HOLD time is still 0ns.***)

**D_H_LINK <31 . . 16>** (Inputs) The link upper 16 data bits.(**Version 0.2:** ***The SETUP time has changed from 4.5 to 5.3ns min. The HOLD time is still 0ns.***)

**SOC_L_LINK** (Input) The link Start Of Cell signal for the lower 16 data bits.(**Version 0.2:** ***The SETUP time has changed from 4.5 to 5.3ns min. The HOLD time is still 0ns.***)

**SOC_H_LINK** (Input) The link Start Of Cell signal for the upper 16 data bits.(**Version 0.2:** ***The SETUP time has changed from 4.5 to 5.3ns min. The HOLD time is still 0ns.***)

**UP_L_LINK** (Input) A feed to the IPP Maintenance Reg., used to detect the state (good or bad) of the lower 16 data bits.

**UP_H_LINK** (Input) A feed to the IPP Maintenance Reg., used to detect the state (good or bad) of the upper 16 data bits**.**

## Core Signals, OPP to IPP:

**D_OPP<31-0>** (Input) The IPP data connection from the OPP receives 32 bits of data labeled 0 through 31. 32 bits of data are received each clock period.

**SOC_OPP** (Input) The Start Of Cell (SOC) signal from the OPP is received by the IPP. This once per cell time signal is aligned with the first word of each cell and is used to synchronize the data communication between the OPP and the IPP.

**PARI_OPP** (Input) Odd parity over the 32 bit field of the "D_OPP" data. A new parity value is received each clock period.

**CLK_OPP** (Input) A clock signal from the OPP that is phased with the data arriving from the OPP.

## Core Signals, IPP to SE:

**D[SE slice number]_IPP<bit number>** (Output) Each IPP feeds a total of 32 bits to the four bit-sliced SE circuits that create one logical "SE" element. The SE slices are labeled 0 through 3, and the eight bits of data to each SE slice are labeled 0 through 7. Each output group produces a new eight bit data value each CLK clock period.

**CTRL[SE slice number]_IPP<bit number>** (Output) Each IPP feeds a total of 4 bits of control to each of the four bit-sliced SE circuits. To allow fanout of only one, the IPP produces four

identical copies of the four control bits. The four copy sets are labeled 0 through 3, and the four bits within each set are labeled 0 through 3.

**PARI[SE slice number]_IPP** (Output) Each of the four bit-sliced SE circuits receives an odd parity bit over the twelve bit field of the combined "D" (data) and "CTRL" fields delivered to each particular SE circuit. A new parity value is transmitted each clock period.

**GRANT_SE** (Input) While each of the four bit-sliced SE circuits generate a "grant" signal, all four of the signals are identical. Thus the IPP will be connected to only one of the four available signals. The other three will be unconnected. Thus only one "Grant_SE" input pin is required. A new grant signal is received each cell clock period. (Once every sixteen clock periods.)

## Other Core Signals:

**CLK** (Input) Input clock to the IPP chip.

**CELL_CLK** (Input) The IPP chip receives a cell clock signal that has a period sixteen times that of the CLK signal. (The form of the CELL_CLK signal is one CLK clock period high, fifteen CLK clock periods low.) The CELL_CLK, signal is the only signal that must meet a setup and hold relationship with every cycle of the CLK signal.

**RESET** (Input, asserted low) The IPP chip receives a reset signal that must meet a setup and hold time relationship with the CLK transition two CLK cycles before the CLK transition for which the CELL_CLK is high. Circuit simulations have shown that the reset signal asserted for 160 clock periods (or more) is adequate for proper circuit operation.

**RESET_REQ** (Output, pull down only, asserted low) The gigabit switch reset circuit is a "wired or" of a reset signal generated at power-up, a reset from a push button switch, and the RESET_REQ signal that can be generated by any IPP circuit (With its CTRL_EN input enabled.) in response to an incoming control cell. The "wired or" reset signal is then synchronized with the core Clock and Cell Clock signals in circuits external to the custom ICs (IPP, SE , and OPP) and distributed to all the switch IC elements as the "RESET" signal. To assure that the RESET_REQ signal is recognized by the following external circuits, the RESET_REQ is asserted by a control cell, and de-asserted by the RESET signal.

**CTRL_EN** (Input) The IPP chip can be configured to accept or ignore control cells delivered at its input port. Circuit simulations have shown that the CTRL_EN signal set for 160 clock periods prior to the removal of RESET is adequate for proper circuit operation.

**CLR_ERR** (Bidirectional, asserted low) The IPP CLR_ERR signal is a bidirectional signal. Via ATM control cells, any IPP circuit can assert CLR_ERR. (CLR_ERR is asserted for at least 32 cell periods.) The rest of the IPP circuits in the switch, along with the OPP and the SE circuits, would then receive that CLR_ERR signal. The CLR_ERR signal clears all error flags in the switch without halting operation of the switch. The actions of the CLR_ERR signal are a sub-set of the actions of the RESET signal. Any error flag cleared by CLR_ERR is also cleared by RESET. The CLR_ERR (received) signal has the same setup and hold time relationship with the CELL_CLK signal as the RESET signal. Circuit simulations have shown that this signal asserted for 160 clock periods (or more) is adequate for proper circuit operation.

**C_CLK_TAP<bit number>**[1] (Input) The timing relationship between the CELL_CLK and the outgoing cell data to the core of the switch is set with this four bit field. Circuit simulations have shown that setting these four bits 160 clock periods prior to the end of the RESET period is adequate for proper circuit operation. The four signals are typically connected to physical switches or jumpers. CC_TAP = 0000 (binary) sets the timing relationship between the outgoing cell and the CELL_CLK such that the first word of a cell is transmitted at the output of the IPP chip on the clock transition following the one for which the CELL_CLK is positive. (See the timing diagrams in Figure 4 for a more detailed timing relationship between the data and the CELL_CLK.) CC_TAP = 0001 (binary) sets the timing relationship such that the first word of a cell is transmitted one CLK period later, etc.

## Test Signals:

For normal operation, all test signal outputs should be left unconnected. All test signal inputs should be tied off as indicated. A brief description of each test signal is included as a reference. Little attention was given to timing as the tests signals were added. The test signals are primarily intended as aids to chip testing at 1MHz. At 120Mhz, some of these test signals may not even switch.

**ALL0** (Output). High when all 32 bits to the reformater are "zero". Used to help test the cell store rams.

**ALL1** (Output). High when all 32 bits to the refomater are "one". Used to help test the cell store rams.

**ALL0BUT1** (Output) High when the LSB of the 32 bit bus to the reformater is "one" and the rest of the bits are "zero". Used to help test the cell store rams.

**BIST_CLK** (Input) On-chip memory test clock, tie to ground when not in the memory test mode.

**BIST_TEST** (Input) On-chip memory test pin. Tie to ground when not in the memory test mode.

**BIST_RES<2 . . 0>** (Output). To be defined.

**QUIK_TEST<1 . . 0>** (Input) Allows simulator and slow clock testing. Tie both inputs to ground when not testing.

**TEST_IPP<49 . . 0>** (Output). There are 50 test outputs with names **TEST_IPP<0>** through **TEST_IPP<49>**. Their names, then the signal name and block source of the signal connected to the input of the pad, and then a brief description of each test output follows.

1. These signals were included to compensate for an expected non-integer cell propagation time through the SE. Since the cell propagation time is an integer cell time (16 CLK periods) with the present SE design, CC_TAP is set to zero in the present switch.

**TEST_IPP<0 > is pad "SOC_H_DSKW_T"** from the RFRM_DSKW block. The signal is clocked by the STRB_L_LINK signal.

This is a delayed version of the higher 16 bits SOC_H_LINK input signal. It is an output of the RFRM_DSKW block, and when the IPP chip's link is in 32 bit mode and the RFRM_DSKW has "hunted" successfully, this signal should be high at exactly the same time as SOC_L_DSKW_T.

**TEST_IPP<1> is pad "SOC_L_DSKW_T"** from the RFRM_DSKW block. The signal is clocked by the STRB_L_LINK signal.

A delayed version of the lower 16 bits SOC_L_LINK input signal. It is an output of the RFRM_DSKW.

**TEST_IPP<2> is pad "LINK_LOCK_T"** from the RFRM_DSKW block. The signal is clocked by the STRB_L_LINK signal.

This signal is often high when the RFRM_DSKW has successfully completed hunting. It is low during reset, and also before the RFRM_DSKW has completed hunting, and sometimes it is low when the RFRM_DSKW had a lock previously, but then lost it. See RFRM_DSKW VHDL code comments for the exact conditions.

**TEST_IPP<3> is pad "REQ_RFRM_T"** from the RFRM block. This signal is clocked by the STRB_L_LINK signal.

This is high for one clock period near the time that the last word of a cell is sent from the RFRM to the CSTR. There is no pulse for cells that are discarded by the RFRM.

**TEST_IPP<4> is pad "CONTROL_RF_T "** from the RFRM block. This signal is clocked by the STRB_L_LINK signal.

This signal indicates whether the cell sent by the REQ_RFRM_T pulse is a control cell (1) or a data cell (0). This signal is only examined by the CSTR on the rising edge of STRB_L_LINK when the REQ_RFRM_T pulse is high.

**TEST_IPP<5> is pad "RXCC_RFRM_T"** from the RFRM block. This signal is clocked by the CLK signal. Test signals 5 through 10 are all copies of signals sent from the RFRM to the MREG, mostly so that the MREG can maintain counters and error flags. All of them change once per internal cell time (16 clock periods of CLK).

RXCC is high for one cell time for each link cell received that has good HEC and is not an ATM unassigned cell.

**TEST_IPP<6> is pad "BADSIGCELL_T"** from the RFRM block. This signal is clocked by the CLK signal.

This signal is high for one cell time for each link cell received that is marked "discard" in Figure 16 of the , "ATM cell header fields for different cell types, by ITU", of the System Architecture Document (except for unassigned cells).

**TEST_IPP<7> is pad "BADCCELL_R_T"** from the RFRM block. This signal is clocked by the CLK signal.

This signal is high for one cell time for each link cell received that is a control cell (VPI=0, VCI=32) when the CTRL_EN option pin is disabled.

**TEST_IPP<8> is pad "BADHEC_RFR_T"** from the RFRM block. This signal is clocked by the CLK signal.

This signal is high for one cell time for each link cell received that has bad HEC.

**TEST_IPP<9> is pad "HLE_RFRM_T"** from the RFRM block. This signal is clocked by the CLK signal.

This signal is high when the link is now up, and it has been up continuously for a number of cell times equal to the Hardware Re-enable Time maintenance register field.

**TEST_IPP<10> is pad "SLETIMEOUT_T"** from the RFRM block. This signal is clocked by the CLK signal.

This signal is high for one cell time when HLE_RFRM_T changes from low to high, and it has been over Software Carrier Loss Time internal cell times since the last time that HLE_RFRM_T was high (unless Software Carrier Loss Time is 0, in which case this signal will never be asserted).

**TEST_IPP<11> is pad "CELLPRES_C_T"** from the CSTR block. This signal is clocked by the CLK signal.

This signal is high for one clock period to indicate to the RCB that a cell is present on the other data pins from the CSTR to the RCB.

**TEST_IPP<12 . . 17> are pads " PTR_RCB_T<0 . . 5>"** from the CSTR block. These signals are clocked by the CLK signal.

This is the 6 bit pointer value assigned to the cell that the CSTR is now sending to the RCB.

**TEST_IPP<18> is pad "PTRAVAIL_M_T"** from the CSTR block. This signal is clocked by the CLK signal.

This signal goes low if the CSTR ever runs out of pointers in its free space list, indicating that all of its 64 cell capacity is used. In correct operation of the chip, this should never happen, because the entire control path of the switch can hold at most 16 + 32 + 2 + about 10 = about 60 cells.

**TEST_IPP<19> is pad "DISC_REQ_R_T"** from the RCB block. This signal is clocked by the CLK signal.

This is high for one clock period whenever the RCB discards a cell due to congestion.

**TEST_IPP<20> is pad "RCBOVF0_RC_T"** from the RCB block. This signal is clocked by the CLK signal.

This signal is high for one cell time whenever the RCB discards a cell with CLP=0 (high priority) due to the buffer being completely full.

**TEST_IPP<21> is pad "RCBOVF1_RC_T"** from the RCB block. This signal is clocked by the CLK signal.

This signal is high for one cell time whenever the RCB discards a cell with CLP=1 (low priority) due to congestion.

**TEST_IPP<22> is pad "CONG_RCB_T"** from the RCB block. This signal is clocked by the CLK signal.

This signal is high during every cell time when the RCB contains more cells than the RCB Discard Threshold maintenance register field.

**TEST_IPP<23> is pad "DATA_RCB_T"** from the RCB block. This signal is clocked by the CLK signal.

This signal is high during every cell time that the RCB is presenting a non-idle cell on its outputs to the RCV circuit.

**TEST_IPP<24> is pad "SOC_DSKW_T"** from the MREG_DSKW block. This signal is clocked by the CLK signal.

This is a delayed version of the SOC_OPP signal, after it has passed through the skew compensation circuit on the recycling path. It is a copy of the SOC signal sent to the MREG, high at the same time as the first word of a recycling cell is sent to the MREG.

**TEST_IPP<25> is pad "RCYC_LOCK_T"** from the MREG_DSKW block. This signal is clocked by the CLK signal.

This is similar to the LINK_LOCK_T signal, except it is for the recycling path skew compensation circuit.

**TEST_IPP<26> is pad "SLE_MREG_T"** from the MREG block. This signal is clocked by the CLK signal.

This signal is short for "Software Link Enable". It reflects the contents of the 1 bit field of that name inside of the maintenance register field, and is a copy of a signal sent to the RFRM.

**TEST_IPP<27> is pad "SOC_MREG_T"** from the MREG block. This signal is clocked by the CLK signal.

This signal is high for one clock period once every 16 clock periods, at a fixed delay after the SOC_DSKW_T pulse appears. It indicates the time when 35 other data signals from the MREG to the CYCB are valid. It is asserted whether the cell is discarded by the MREG or not.

**TEST_IPP<28> is pad "REQ_MREG_T"** from the MREG block. This signal is clocked by the CLK signal.

This signal is high for one clock period near the last word of a cell sent from the MREG to the CSTR. It is only asserted if the MREG does not discard the cell.

**TEST_IPP<29> is pad "RLE_MREG_T"** from the MREG block. This signal is clocked by the CLK signal.

This signal reflects the contents of the "Recycling Link Enable" field in the maintenance register. It is high if the MREG accepts data cells, or low if the MREG discards data cells.

**TEST_IPP<30> is pad "DATA_CYCB_T"** from the MREG block. This signal is clocked by the CLK signal.

Oddly enough, this appears to be identical to REQ_MREG_T. Auugh! A wasted pin!

**TEST_IPP<31> is pad "DATA_FULL_T"** from the CYCB block. This signal is clocked by the CLK signal.

This signal is a copy of the DATA_FULL_CYCB signal sent from the CYCB to the MREG to indicate that the FIFO that can hold 16 data cells is full.

**TEST_IPP<32> is pad "CONTROL_FU_T"** from the CYCB block. This signal is clocked by the CLK signal.

This signal is a copy of the CONTROL_FULL_CYCB signal sent from the CYCB to the MREG to indicate that the FIFO that can hold 2 control cells is full.

**TEST_IPP<33> is pad "GRANT_RCV_T"** from the CYCB block. This signal is clocked by the CLK signal.

This is a copy of the signal GRANT_RCV_CYCB sent from the CYCB to the RCV circuit, which the RCV uses to choose whether the cell from the RCB or the CYCB is passed through.

**TEST_IPP<34> is pad "REQ_VXTC_T"** from the VXTC block. This signal is clocked by the CLK signal.

This signal is high for one cell time when a new cell arrives at the VXTC for processing. It is asserted whether the cell is discarded or propagated through the VXTC.

**TEST_IPP<35 . . 40> are pads "PTR_VXTC_T<0 . . 5>"** from the VXTC block. These signals are clocked by the CLK signal.

This is the 6 bit pointer value for the cell requested by the VXTC at the REQ_VXTC_T pulse.

**TEST_IPP<41> is pad "GRANT_CYCB_T"** from the VXTC block. This signal is clocked by the CLK signal.

This signal is a copy of the GRANT_CYCB_VXTC signal sent from the VXTC to both the CYCB and RCB. It is high when the "input holding area" of the VXTC is able to accept another cell, and indicates that one of the CYCB and RCB should send a cell, if they have one available. This signal is low during reset and hardware initialization of the VXTC.

**TEST_IPP<42> is pad "VXIOR_VXTC_T"** from the VXTC block. This signal is clocked by the CLK signal.

This signal is asserted high for one cell time when the VXTC discards a data cell because its VPI was out of range, as determined solely by the value of the VP Count maintenance register field, or because its VCI was out of range, which is only true if the VPT bit is set in the VP entry for the cell, and the VCI is too large, as determined by the size of the whole table (1024) and the VP Count.

**TEST_IPP<43> is pad "CS0_DISC_V_T"** from the VXTC block. This signal is clocked by the CLK signal.

This signal is asserted high for one cell time when the VXTC discards a data cell because its table entry assigns it a CS value of 0, and the RCB was congested at least once within the last RCB Discard Hold Duration cell times.

**TEST_IPP<44> ia pad "DATA_RCV_T"** from the VXTC block. This signal is clocked by the CLK signal.

This signal is high for one cell time whenever the cell in the "input holding area" of the VXTC is not an idle cell. If this signal is asserted for several cell times in a row, it could be because the same cell is sitting there without advancing, or it could be because several non-idle cells have streamed through this area back to back.

**TEST _IPP<45 . . 49> are pads with their inputs grounded**. These pads are unused, but were not deleted from the pad ring.

## Power and Ground Signals:

The OPP chip has a set of 3.3V power pads that supply power to the core of the chip, a set of 3.3V power pads that supply power to the pad I/O circuits, and a set of four 5.0V power pads that are used in conjunction with the TTL input signals for the port interface.

**Core PWR** 3.3V pads that supply power to the core of the chip.

**Periphery PWR** 3.3V pads that supply power to the chip pads. (The Periphery of the chip).

**TTL PWR** 5.0V pads that provides the input bias voltage for the TTL input pads.

The OPP chip has a set of ground pads that feed the core of the chip, a set of pads that feed the pads themselves, and a set of ground pads that are used in conjunction with the TTL input signals for the port interface.

**Core GND** Ground pads that feed the core of the chip.

**Periphery GND** Ground pads that feed the chip pads themselves. (The Periphery of the chip).

**TTL GND** TTL input ground pads.

## Chip Physical Specifications:

The signal names used in Figure 1 are the same signal names used in the IPP_TOP.pin file that is generated as part of the design flow for each circuit. The IPP_TOP.pin file for the Input Port Processor chip is attached as Appendix A. The IPP_TOP.pin file lists the chip SIGNAL and 5.0V TTL power pads in the order they appear around the edge of the chip (TTL power pads are included with the signal pins since they are not connected to the package power plane as are the other (3.3V core and periphery) power pads). The 3.3V power and all the ground pads are then listed. The "PAD CENTRE COORDINATES" column must be used to determine the interleaving of power and ground pads with signal pads. The "BND PIN" column of the IPP_TOP.pin file lists the package cavity bonding land number. The SIGNAL and 5.0V TTL power bonding land numbers, numbers 1 through 256, map to the ES2 299 pin PGA package pin designations, "A1" through "X20" (See Appendix B ) The 299 PGA package used to house the SE chip has power and ground planes within the package. Thus the 3.3V power and all the ground PINS on the PGA package do not map directly to the power and ground PADS on the chip. As detailed in Appendix B, there are a total of 21 power and 22 ground pins on the package. (Note, from Figure 1, that there are a total of 57 power and 56 ground PADS on the chip.) The IPP chip layout, Figure 3, indicates the coordinates on the chip which are used with the Table of Appendix A to identify the position of each pad.

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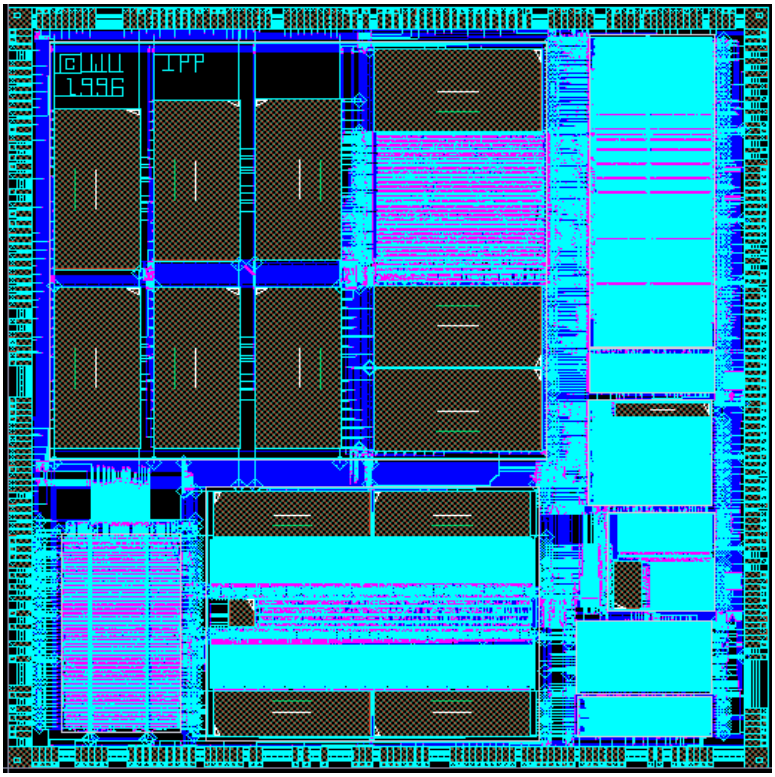
7150, 6832 7150, -6832




-7150, 6832 -7150, -6832

**Figure 3**

**Input Port Processor with Coordinate System used in Appendix A shown.**

## SIGNAL TIMING:

The general timing values and conditions for all three GigaBit Switch chips (SE, IPP, OPP) are given in ARL-96-4. Information specific to the IPP is given here.

### INPUT SIGNAL TIMING FROM OPP:

These IPP chip input circuits include clock-to-data deskewing circuits which adjust the timing of the data path, relative to the clock, regardless of the OPP to IPP Cell_CLK timing relationship.

## GENERAL INPUT SIGNAL TIMING:

CLK: up to 120MHz, 40%-60% worst case duty factor, rise and fall times < 2ns.

CELL_CLK: setup time =2.8ns, hold time = -0.9ns

RESET, CLR_ERR: clocked on the positive clock transition two transitions before the transition for which the CELL_CLK signal is high. Detailed timing is shown in Figure 5. (Setup time = 0ns, Hold time = 2.9ns.)

GRANT_SE: clocked on the positive edge of the eight clock period associated with the period the CELL_CLK signal is high. Detailed timing shown in Figure 4. (Setup time =1.6ns, Hold time = 0.9ns)

D_OPP, SOC_OPP, and PARI_OPP, relative to CLK_OPP: A clock signal is passed from the OPP to the IPP along with the 34 bits of data and control. The 32 bits are strobed into Flip-Flops by the FALLING EDGE of the CLK_OPP signal. Then the output of these Flip_Flops are phase aligned with the IPP clock signal. (Setup time = 1.2ns, Hold time = 1.6ns) Detailed timing shown in Figure 6.

## OUTPUT SIGNAL TIMING

With the exception of the RESET_REQ and CLR_ERR signals, all outputs may exhibit new values each clock period. The RESET_REQ signal is an asynchronous output that, once asserted, remains asserted until the RESET input is asserted. The CLR_ERR signal is asserted for at least 255 cell periods. Detailed timing is shown in Figure 4.

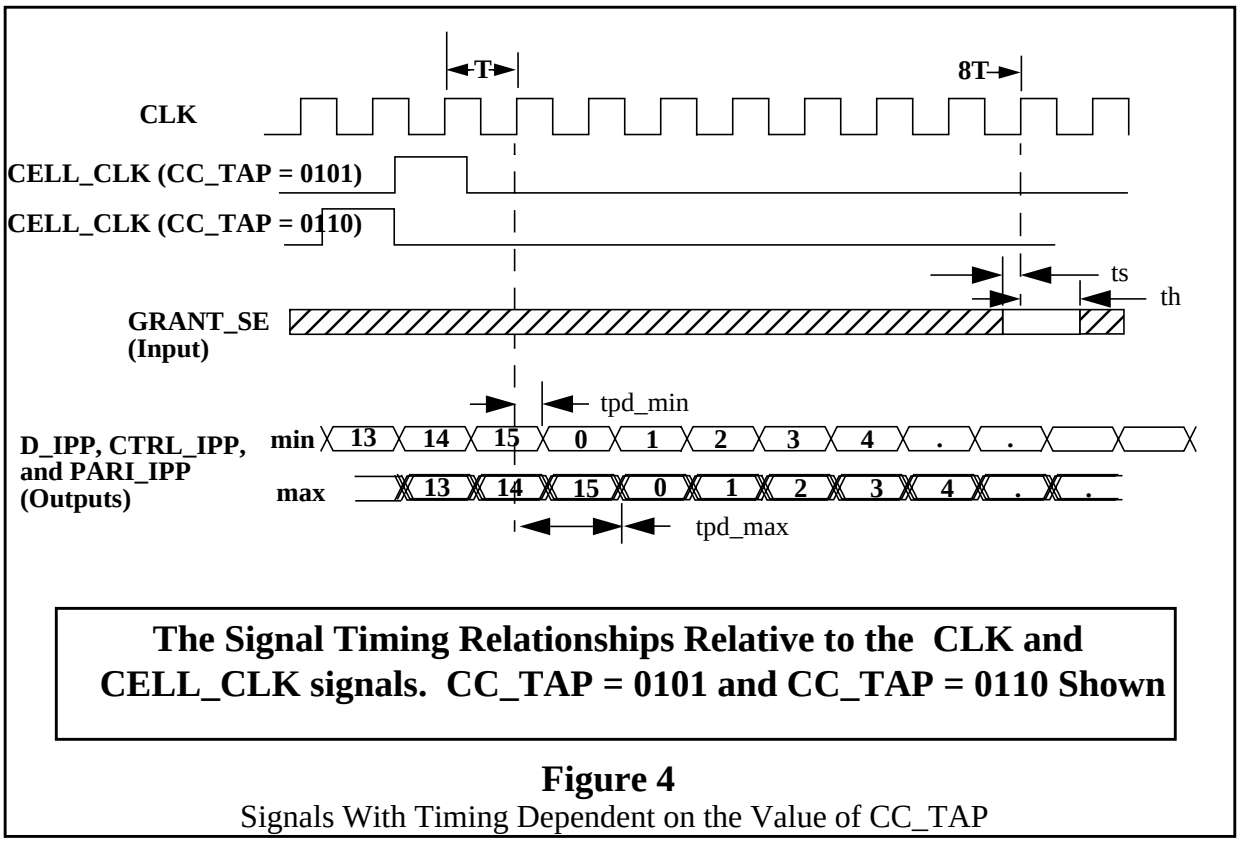



**Figure 4**
Signals With Timing Dependent on the Value of CC_TAP

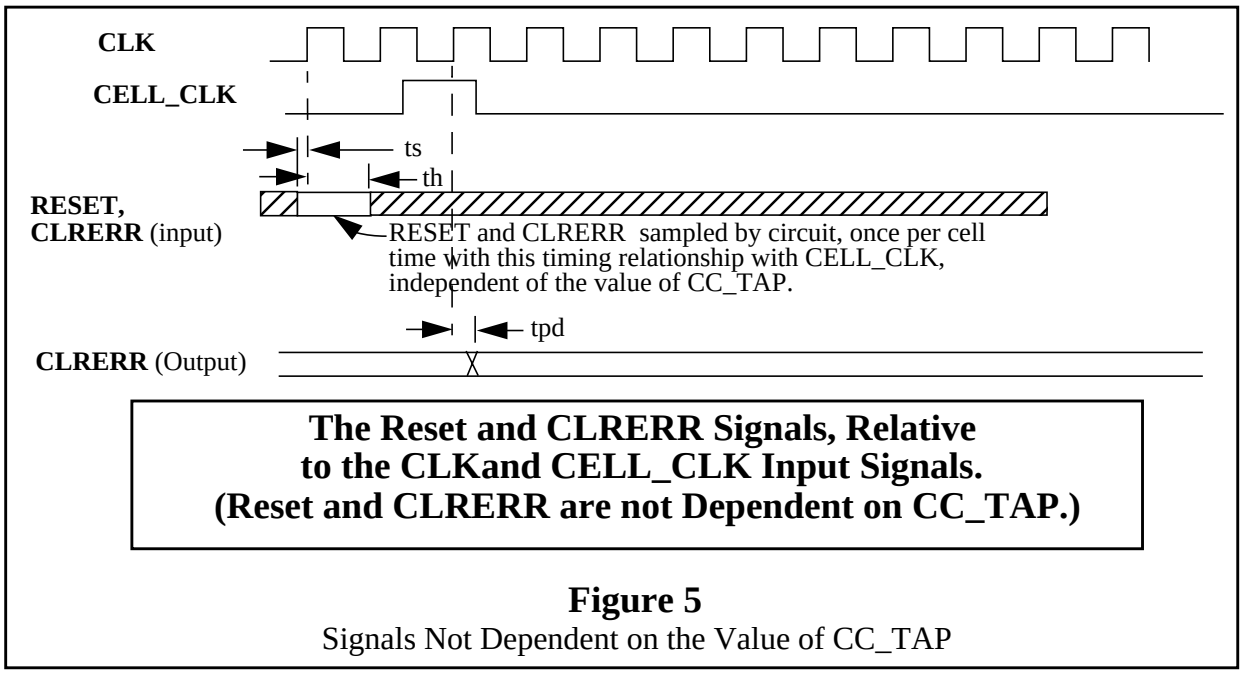
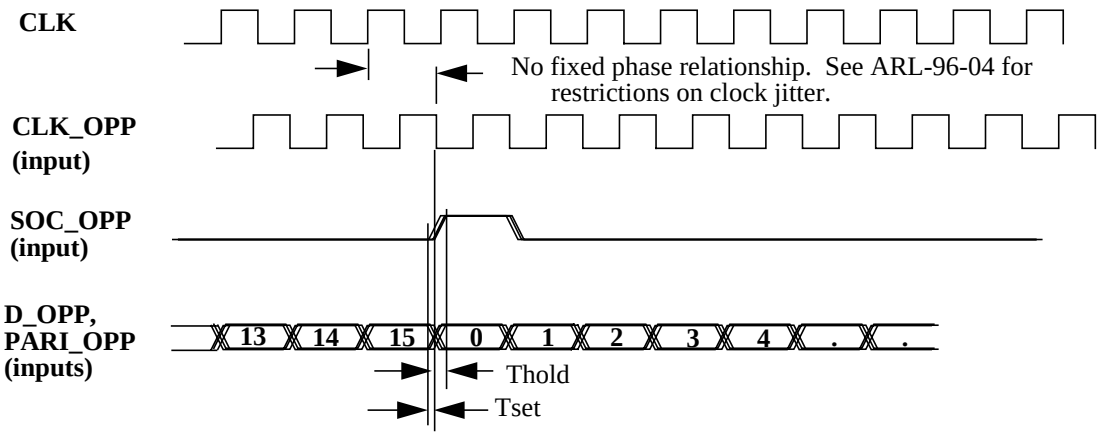



**Figure 5**
Signals Not Dependent on the Value of CC_TAP




**The OPP to IPP Signals , Relative to Each Other and to the IPP CLK Signal.**

**Figure 6**
OPP to IPP Signal Timing

# Appendix A

(Print out of the pin_package_rpt_APPENDIX_A.txt file, this directory)
(pages A-1 through A-10)

# Appendix B

(Copy of 299 PGA pinout from data book)
(Page 35 of Atmel/ES2 Package Selector Guide, Rev. AG4-AO02/J, Oct. 1994)

# Appendix C

(Copy of Bonding Diagrams Submitted to Atmel/ES2)
(3 pages )

The package used for the IPP chip is a 299 pin PGA package with an internal power and ground plane. The use of the power and ground planes in the package force a fixed package pin assignment for the package power and ground outside pins. Inside the bond cavity, the power and the ground planes each appear as fixed location bond land *regions* around the bond cavity. These bonding regions vary in size from an area large enough to support bonds to seven power or ground chip pads, to an area the same size as the signal bonding lands. Also, the placement of a power or ground pad around any part of the periphery of the chip that is not lined up with the appropriate power or ground region can not be effectively fed from the package. The inductance of a signal pin circuit is so much higher than the inductance of a power or ground plane connection circuit that there is little value in making a power or ground connection using a signal pin circuit. However, to effectively feed the core circuit from the pad ring power, it is often helpful to place a power or ground pad in the pad ring and use this pad to only feed power to the core. Thus chip designs end up with power and ground pads that are not intended to be bonded. The Atmel/ES2 software tool set does not support this package very well. Thus there is some hand drawn work required to complete the bonding diagrams. To assure there are no errors in the hand drawn work, there are four pages of bonding diagrams.

The three pages of bonding diagrams are attached as this Appendix C. The first page shows all the bonds on one diagram. The package cavity is a two tier design. The bond connections to just the bottom(inside) tier is shown on the second page, and the bonds to just the top (outer) tier is shown on page three.