Working Note ARL-96-07

OPP Signal Description

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This document provides the Input and Output signal description, position, and timing for the Output Port Processor (OPP) integrated circuit used in the Washington University Gigabit Switch described in "System Architecture Document for GIGABIT SWITCHING TECHNOLOGY, Version 3.1, Working Note ARL-94-11, by Jonathan S. Turner and staff.

OUTPUT PORT PROCESSOR(OPP) I/O DIAGRAM

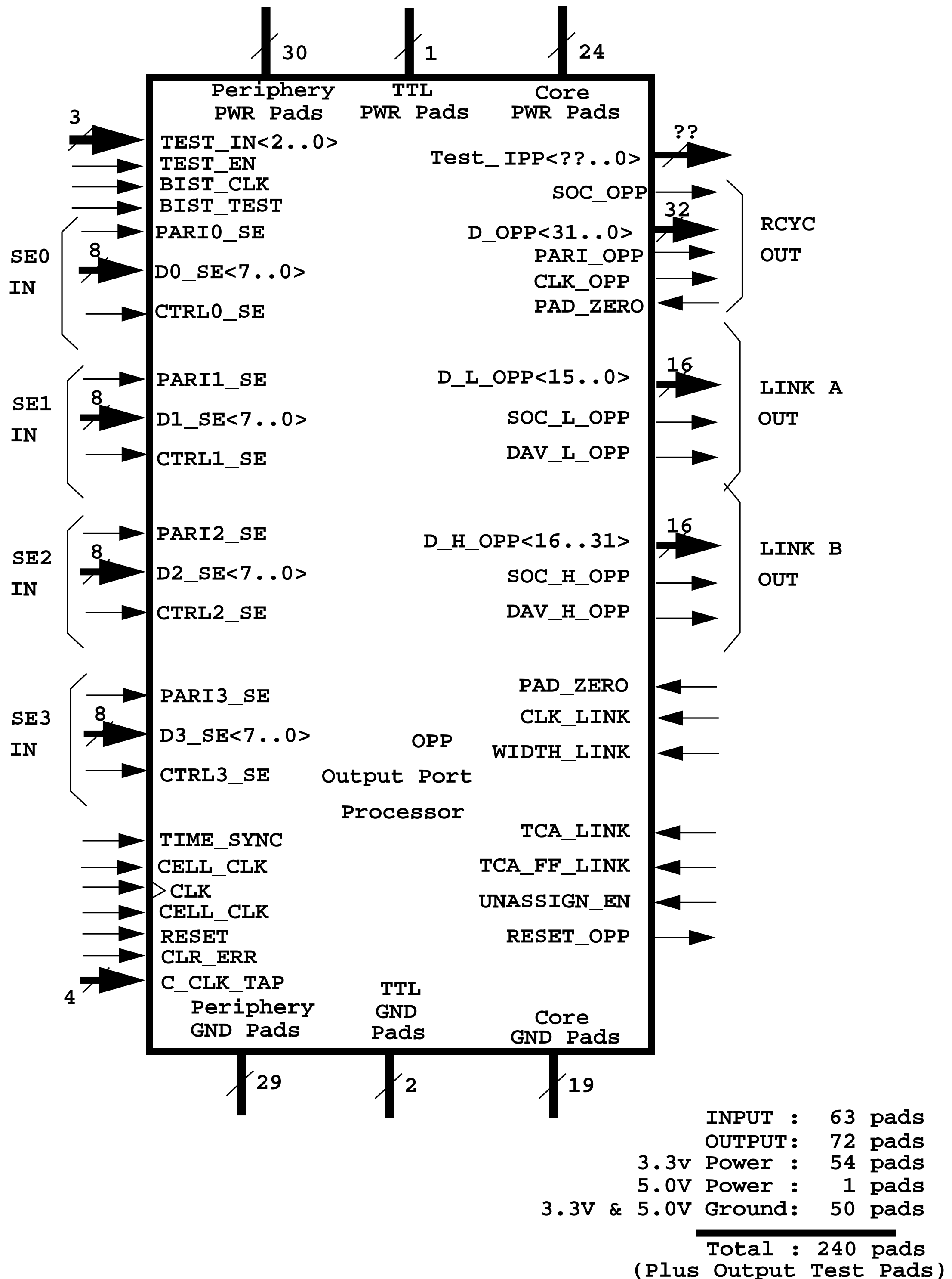

Figure 1
Output Port Processor (OPP) chip I/O Diagram

Signal Descriptions:

The OPP provides an interface between the ATM port with its associated link clock, and the switch core with its associated core clock. The signaling within the switch core utilizes a clock-to-data deskewing circuit and a high (120mhz) clock rate. The signaling associated with the ATM port is described in great detail in "The Gigabit Switch Link Interface Specification" by W. D. Richard, Version 4.1, Working Note ARL-94-17, Jan. 18, 1996. The ATM port signals will only be listed in this document. The signals associated with the switch core, and the test signals associated with the OPP will be described in this document.

Port Interface Signals: (Described in W. D. Richard)

WIDTH_LINK (Input) A static level, sets port data interface to 16 or 32 bit data word.
UNASSIGN_EN (Input) Static level, Enables transmission of Unassigned Cells during idle cell periods.
CLK_LINK (Input) The link "clock".
TCA_LINK (Input) Send another cell enable signal, intended for use with early UTOPIA devices.
TCA_FF_LINK (Input) Send another cell enable signal. Used for all but early UTOPIA devices.
D_L_OPP <15 . . 0> (Outputs) The link lower 16 data bits.
D_H_OPP <16 . . 31> (Outputs) The link upper 16 data bits.
SOC_L_OPP (Output) The link Start Of Cell signal for the lower 16 data bits.
SOC_H_OPP (Output) The link Start Of Cell signal for the upper 16 data bits.
DAV_L_OPP (Output) The Data AVailable signal for the lower 16 data bits.
DAV_H_OPP (Output) The Data AVailable signal for the upper 16 data bits.
RESET_OPP (Output) A buffered RESET feed that reflects the switch RESET signal. This signal is not synchronized with the link clock (The "CLK_LINK").
PAD_ZERO (Input) Forces a particular pattern (all zeros) into an unused byte(s) of the 16 and 32 bit wide utopia header formats. Needed by some utopia devices. A static level.

Core Signals, OPP to IPP:

D_OPP<31-0> (Output) The OPP data connection to the IPP transmits 32 bits of data labeled 0 through 31. The OPP to IPP connection transmits 32 bits of data each clock period.
SOC_OPP (Output) The Start Of Cell (SOC) signal from the OPP is received by the IPP. This once per cell time signal is aligned with the first word of each cell and is used to synchronize the data communication between the OPP and the IPP.
PARI_OPP (Output) Odd parity over the 32 bit field of the "D_OPP" data. A new parity value is transmitted every clock period.
CLK_OPP (Output) A clock signal to the IPP that is phased with the data sent to the IPP.

Core Signals, OPP from SE:

D[SE slice number]_SE<bit number> (Input) Each OPP receives a total of 32 bits from the four bit-sliced SE circuits that create one logical "SE" element. The SE slices are labeled 0 through 3, and the eight bits of data from each SE slice are labeled 0 through 7. Each group receives a new eight bit data value each core clock period.
CTRL[SE slice number]_SE (Input) Each OPP receives a total of 4 bits of control from the four bit-sliced SE circuits. Bit 0 is received from SE slice 0, bit 1 is received from SE slice 1, etc. Many of the SE CTRL outputs are not used at the interface to the OPP, but would be used in a multi-stage switch for connection from SE chip to SE chip. A new control value is received

each clock period.

PARI[SE slice number]_SE (Input) Each of the four bit-sliced SE circuits transmits Odd parity over the twelve bit field of the combined "D" (data) and "CTRL" fields delivered from each particular SE circuit. A new parity value is received each clock period.

Global Signals:

CLK (Input) Input clock to the OPP chip.

CELL_CLK (Input) The OPP chip receives a cell clock signal that has a period sixteen times that of the CLK signal. (The form of the CELL_CLK signal period is one CLK clock period high, fifteen clock CLK periods low.) The CELL_CLK signal is the only signal that must meet a setup and hold relationship with every cycle of the CLK signal.

RESET (Input, asserted low) The OPP chip receives a reset signal that must meet a setup and hold time relationship with respect to the CLK transition two CLK cycles before the CLK transition for which CELL_CLK is high. Circuit simulations have shown that the reset signal asserted for 160 clock periods (or more) is adequate for proper circuit operation.

CLR_ERR (Input) The CLR_ERR signal clears all error flags in the switch without halting operation of the switch. The actions of the CLR_ERR signal are a sub-set of the actions of the RESET signal. Any error flag cleared by CLR_ERR is also cleared by RESET. The CLR_ERR signal has the same setup and hold time relationship with the CELL_CLK signal as the RESET signal. Circuit simulations have shown that this signal asserted for 160 clock periods (or more) is adequate for proper circuit operation.

C_CLK_TAP<bit number>[1] (Input) The timing relationship between the CELL_CLK and the received cell data from the core of the switch is set with this four bit field. Circuit simulations have shown that setting these four bits 160 clock periods (or more) prior to the end of the RESET period is adequate for proper circuit operation. The four signals are typically connected to physical switches or jumpers. CC_TAP = 0000 (binary) sets the timing relationship between the outgoing cell and the CELL_CLK such that the first word of a cell is received at the input to the OPP chip on the clock period the CELL_CLK is positive. (See the timing diagrams in Figure 3 for a more detailed timing relationship between the data and the CELL_CLK.) CC_TAP = 0001 (binary) sets the timing relationship such that the first word of a cell is transmitted one CLK period later, etc.

TIME_SYNC (Input) This signal synchronizes the time stamp value in the OPP and is intended to be used when “hot board swapping” is designed into the Gigabit Switch. When a board with a OPP on it is replaced in an operating system, the value in the OPP time stamp resister must be reset to the same value that is currently in the rest of the OPPs and IPPs in the switch. To accomplish this re-synchronization, the OPP contains a 33 bit shift register circuit. The input to the shift register is the TIME_SYNC signal. The value of the TIME_SYNC signal is shifted in once per cell time, with the same timing relationships used by the reset - cell clk signaling. When the 33ed bit of the OPP shift register is a “one” (electrical high), the lower 32 bits are parallel loaded into the 32 bit time stamp register/counter and the 33 bit shift register is cleared. The

1. These signals were included to compensate for an expected non-integer cell propagation time through the SE. Since the cell propagation time is an integer cell time (16 CLK periods) with the present SE design, CC_TAP is set to zero in the present switch.

master source of the TIME_SYNC signal will be in the same set of circuits that provide the clk, cell clk, and reset signals for the gigabit switch. The TIME_SYNC master source is expected to transmit a one cell time wide “one” signal (a “start” bit), followed by the 32 bit current time stamp value as a serial bit stream, at a rate of one bit per cell time. This bit stream can be sent as often as once every 65 cell times. Providing a 32 bit sequence of all “0”s between the end of one serial bit stream and the “start” bit of the next serial bit stream allows a specification that any OPP will have it’s time stamp register synchronized with the rest of the gigabit switch system in less than 100 cell times. (The maximum sequence is the OPP comming out of reset and just missing a start bit on a time stamp sequence of all zeros with a LSB being a “1” (32 cell times) plus the 32 bit “dead time” sequence of “0” (32 more cell times) plus the 33 cell time sequence of a correct time stamp. Thus a total of 97 cell times maximum after partial reset is removed is needed to assure all OPPs in a system are synchronized again.)

Test Signals:

BIST_CLK (Input) On-chip memory test clock, tie to ground when not in the memory test mode.

BIST_TEST (Input) On-chip memory test pin. Tie to ground when not in the memory test mode.

TEST_EN (Input) This signal enables the test output pins. When TEST_EN is low, all test output pins will be inactive and low.

TEST_IN<2 . . 0> (Input) Three extra inputs that are specified now so that the PC board layout can be finished. These three inputs will be tied to ground in the PC board layout.

TEST_IPP<?? . . 0> (Output). To be defined.

Power Signals:

The OPP chip has a set of 3.3V power pads that supply power to the core of the chip, a set of 3.3V power pads that supply power to the pad I/O circuits, and a 5.0V power pad that is used in conjunction with the TTL input signals for the port interface.

Core PWR 3.3V pads that supply power to the core of the chip.

Periphery PWR 3.3V pads that supply power to the chip pads. (The Periphery of the chip).

TTL PWR 5.0V pad that provides the input bias voltage for the TTL input pads.

The OPP chip has a set of ground pads that feed the core of the chip, a set of pads that feed the pads themselves, and a set of ground pads that are used in conjunction with the TTL input signals for the port interface.

Core GND Ground pads that feed the core of the chip.

Periphery GND Ground pads that feed the chip pads themselves. (The Periphery of the chip).

TTL GND TTL input ground pads.

Chip Physical Specifications:

The signal names used in Figure 1 are the same signal names used in the OPP_TOP.pin file that is generated as part of the design flow for each circuit. The OPP_TOP.pin file for the Input Port Processor chip is attached as Appendix A. The OPP_TOP.pin file lists the chip SIGNAL and 5.0V TTL power pads in the order they appear around the edge of the chip (TTL power pads are included with the signal pins since they are not connected to the package power plane as are the other (3.3V core and periphery) power pads). The 3.3V power and all the ground pads are then listed. The "PAD CENTRE COORDINATES" column must be used to determine the interleaving of power and ground pads with the signal pads. The "BND PIN" column of the OPP_TOP.pin file lists the package cavity bonding land number. The SIGNAL and 5.0V TTL power bonding land numbers, numbers 1 through 256, map to the ES2 299 pin PGA package pin designations, "A1" through "X20" (See Appendix B) The 299 PGA package used to house the SE chip has power and ground planes within the package. Thus the 3.3V power and all the ground PINS on the PGA package do not map directly to the power and ground PADS on the chip. As detailed in Appendix B, there are a total of 21 power and 22 ground pins on the package. (Note, from Figure 1, that there are a total of <<XX>> power and <<YY>> ground PADS on the chip.) The OPP chip layout, Figure 2, indicates the coordinates on the chip which are used with the Table of Appendix A to identify the position of each pad.

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7000, 7000 7000, -7000

TO BE ADDED

-7000, 7000 -7000,7000

Figure 2

Output Port Processor with Coordinate System used in Appendix A shown.

SIGNAL TIMING:

The general timing values and conditions for all three GigaBit Switch chips (SE, IPP, OPP) are given in ARL-96-4. Information specific to the OPP is given here.

INPUT SIGNAL TIMING FROM SE:

The OPP chip input circuits include clock-to-data deskewing circuits which adjust the timing of the data path, relative to the clock, over approximately two clock periods. These circuits significantly increase the traditional signal-timing tolerances.

GENERAL INPUT SIGNAL TIMING:

CLK: up to 120MHz, 40%-60% worst case duty factor, rise and fall times < 2ns.
CELL_CLK: setup time > 1.75ns, hold time > 1.00ns

RESET, CLR_ERR: clocked on the positive clock transition two transitions before the transition for which the CELL_CLK signal is high. Detailed timing is shown in Figure 4.

D_SE, CTRL_SE, and PARI_SE: The general timing, including the relationship between the ATM cell word position relative to CELL_CLK and the value of CC_TAP, is shown in Figure 3. The D_SE, CTRL_SE, and PARI_SE in the data groups indicated below. Detailed timing shown in Figure 3.

Group 1, Dx_SE_0 through Dx_SE_4 (5 bits) -- all relative to Dx_SE_0

Group 2, Dx_SE_5 through Dx_SE_7, CTRLx_SE , and PARIx_SE (5 bits) -- all relative to Dx_SE_5
(Note: this grouping may change.)

OUTPUT SIGNAL TIMING

Detailed timing is shown in Figure 3. The timing details of the output signals associated with the link interface are described in W. Richard.

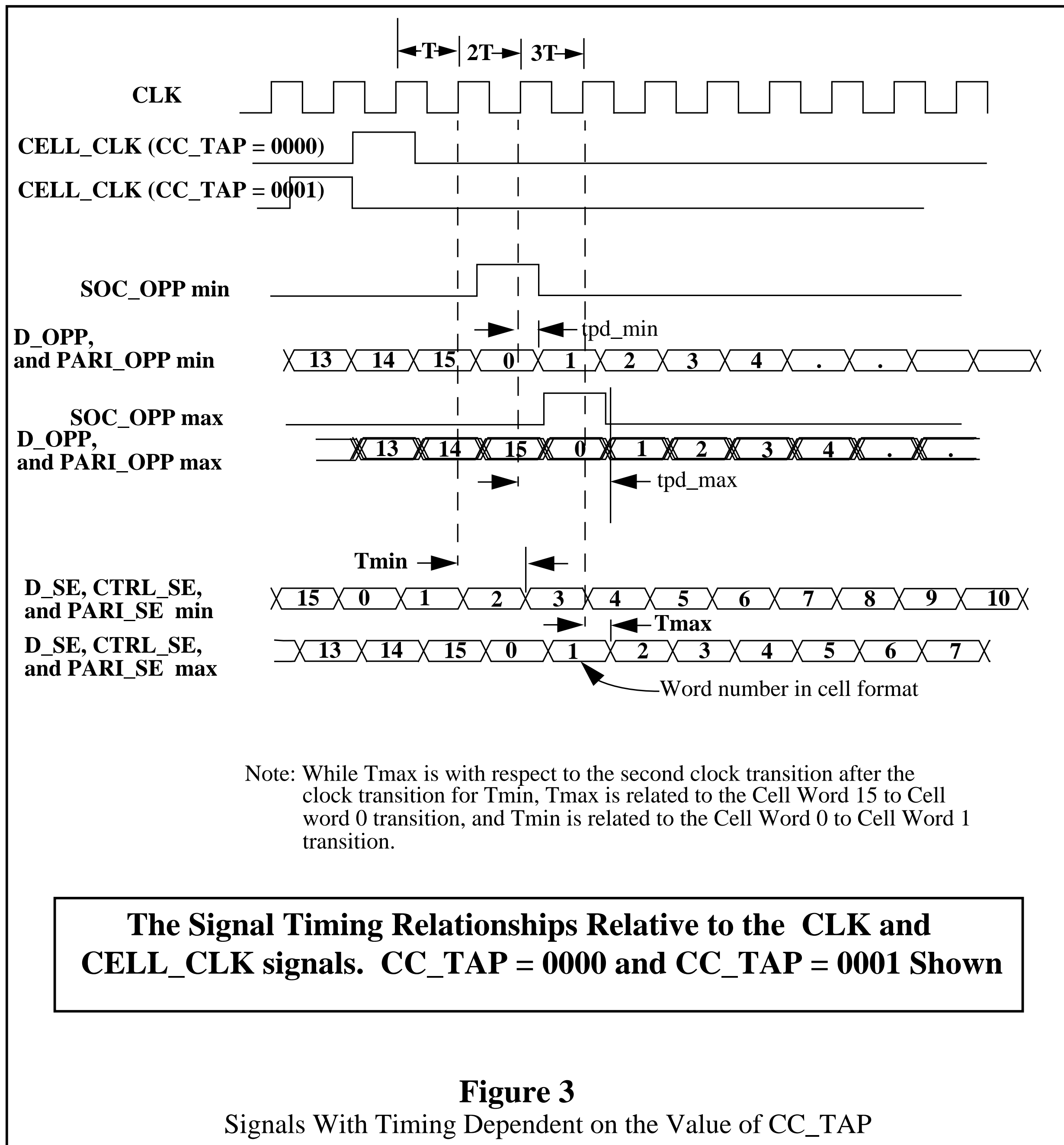


Figure 3
Signals With Timing Dependent on the Value of CC_TAP

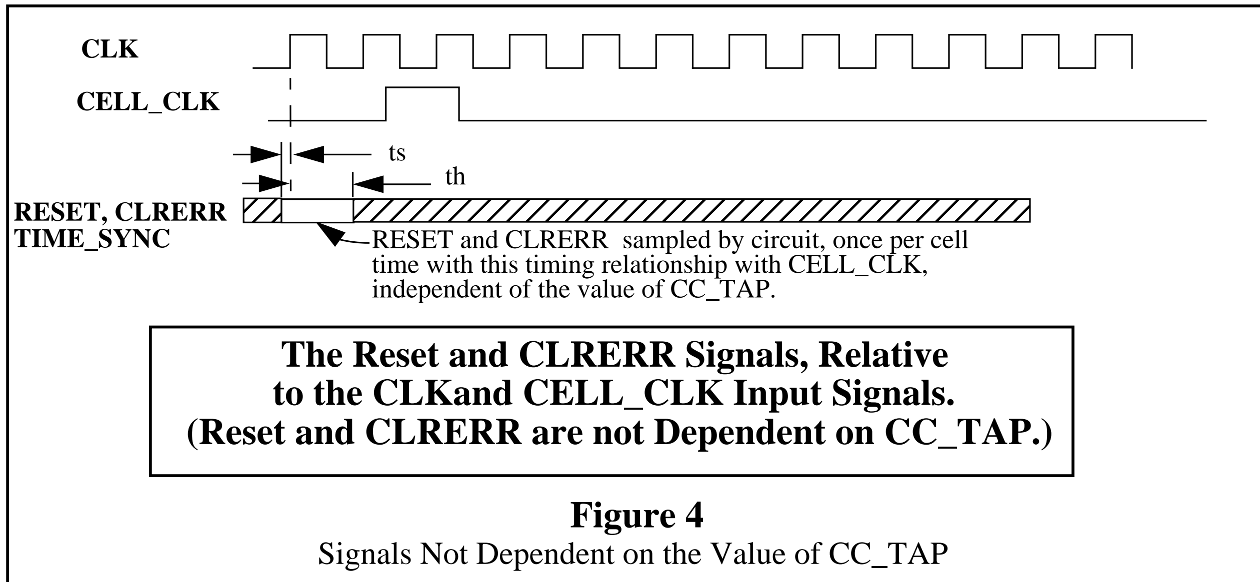
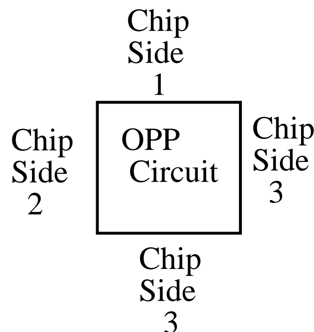


Figure 4
Signals Not Dependent on the Value of CC_TAP

Appendix A

(Print out of the pin_package_rpt_APPENDIX_A.txt file, this directory)
(pages A-1 through A-10)

Until the OPP layout is finished, there is no pin_package_rpt_APPENDIX_A.txt file. Until then, the following table can serve to guide planning for the OPP. The table is designed to show the defined paths between the OPP chip pads, and 299 PGA package bonding lands. This information allows the designer to KNOW the sequence of the signal pads around the OPP chip, to KNOW which of the four edges a particular signal pad is placed, and to ESTIMATE approximately where along a chip edge a particular signal pad is placed based on the knowledge of the placement of the attaching bonding land in the package.(see Appendix B) The power and ground pads are less well defined. The sequential placement and number of the power and grounds in the following table are approximate and *will* be changed as the OPP layout progresses. The PGA package being used has *regions* of power bonding lands, and *regions* of ground bonding lands so that a ground or a power pad placed anywhere adjacent to a region can still be bonded to the package power or ground bonding land. It is possible that, late in the OPP chip layout process, the positions of a power or a ground pad will be moved, one way or the other, past a few signal pads. (Note, the 5 Volt power connections to the chip use package signal pins and thus can not move past other signal pads Only the +3.3 volt and ground pads may move within the regions.) Thus the only way to assure the designed OPP chip will match a new package bonding land pattern is to provide a three-tier bonding land system with two of the tiers being a power ring and a ground ring and the third tier being all the signal connections in the proper sequence and chip edge, or to make an exact physical copy of the targeted two tier PGA package chip cavity. It should be noted that the placement of the test output pads is not included. (The INPUT test pad locations are included.) The number and function of the test output pads is adjusted based design details of each block. Thus the final test pad list is not known until late in the design cycle. The output test pad placements are not critical to chip attachment designs as all output test pads could be left unconnected. Each two pages of the following table covers one edge of the OPP chip: (The four "CRNGNDPY" type pads are the pads that fit in the four corners of the pad ring.)



Signal Name	Package Pin	Bonding land	pad type
GND	-	273	CRNGNDPY(Corner)
GND (GNDCO_P_1)	-	273	GNDCO Chip
GND (GNDPY_P_1)	-	273	GNDPY edge
D3_SE<3>	C3	1	IPS8B 1
--> not connected <--	E5	2	{NO pad}
D3_SE<2>	B3	3	IPS8B
--> un-used <--	E6	4	<space>
D3_SE<5>	C4	5	IPS8B
RSQ_EMP	D6	6	OPS0T
RSQOVF	D5	7	OPS0T
--> un-used <--	E7	8	<space>
D3_SE<4>	B4	9	IPS8B
PARI3_SE	C5	10	IPS8B
Vdd (+3.3V) (PWRCO_P_1)	-	274	PWRCO
CTRL3_SE	B5	11	IPS8B
Vdd (+3.3V) (PWRPY_P_1)	-	274	PWRPY
D3_SE<6>	A5	12	IPS8B
Vdd (+3.3V) (PWRCO_P_2)	-	274	PWRCO
--> un-used <--	C6	13	<space>
Vdd (+3.3V) (PWRPY_P_2)	-	274	PWRPY
D2_SE<0>	B6	14	IPS8B
Vdd (+3.3V) (PWRCO_P_3)	-	274	PWRCO
--> un-used <--	D7	15	<space>
Vdd (+3.3V) (PWRPY_P_3)	-	274	PWRPY
NO_BOND_GNDCO_2			**GNDCO**
D3_SE<7>	A6	16	IPS8B
GND (GNDCO_P_2)	-	258	GNDCO
GND (GNDPY_P_2)	-	258	GNDPY
--> un-used <--	C7	17	<space>
--> un-used <--	E8	18	<space>
D2_SE<2>	B7	19	IPS8B
--> un-used <--	D8	20	<space>
D2_SE<1>	A7	21	IPS8B
--> un-used <--	E9	22	<space>
D2_SE<5>	C8	23	IPS8B
--> un-used <--	D9	24	<space>
D2_SE<3>	B8	25	IPS8B
D2_SE<7>	C9	26	IPS8B
D2_SE<4>	A8	27	IPS8B
CTRL2_SE	C10	28	IPS8B
D2_SE<6>	B9	29	IPS8B
--> un-used <--	E10	30	<space>
PARI2_SE	B10	31	IPS8B
--> un-used <--	D10	32	<space>
GND (GNDPY_P_3)	-	259	GNDPY
GND (GNDPY_P_4)	-	259	GNDPY
Vdd (+3.3V) (PWRPY_P_4)	-	275	PWRPY
Vdd (+3.3V) (PWRCO_P_4)	-	275	PWRCO
Vdd (+3.3V) (PWRPY_P_5)	-	275	PWRPY

Signal Name	Package Pin	Bonding land	pad type	
D1_SE<0>	B11	33	IPS8B	
--> un-used <--	D11	34	<space>	
D1_SE<2>	B12	35	IPS8B	
--> un-used <--	E11	36	<space>	
D1_SE<4>	B13	37	IPS8B	
D1_SE<1>	C11	38	IPS8B	
D1_SE<7>	A14	39	IPS8B	
D1_SE<3>	C12	40	IPS8B	
D1_SE<5>	C13	41	IPS8B	
--> un-used <--	D12	42	<space>	
D1_SE<6>	B14	43	IPS8B	
--> un-used <--	E12	44	<space>	
D0_SE<1>	A15	45	IPS8B	
--> un-used <--	D13	46	<space>	
NOT_RDY	E13	48	OPS0T	
PARI1_SE	C14	47	IPS8B	
CTRL1_SE	B15	49	IPS8B	
GND (GNDPY_P_5)	-	260	GNDPY	
GND (GNDCO_P_3)	-	260	GNDCO	
D0_SE<2>	A16	50	IPS8B	
Vdd (+3.3V) (PWRPY_P_6)	-	276	PWRPY	
--> un-used <--	C15	51	<space>	
Vdd (+3.3V) (PWRCO_P_5)	-	276	PWRCO	
D0_SE<0>	B16	52	IPS8B	
Vdd (+3.3V) (PWRPY_P_7)	-	276	PWRPY	
D0_SE<5>	A17	53	IPS8B	
Vdd (+3.3V) (PWRCO_P_6)	-	276	PWRCO	
--> un-used <--	C16	54	<space>	
Vdd (+3.3V) (PWRPY_P_8)	-	276	PWRPY	
D0_SE<4>	B17	55	IPS8B	
--> un-used <--	D16	56	<space>	
--> un-used <--	D14	57	<space>	
D0_SE<3>	C17	58	IPS8B	
--> un-used <--	E14	59	<space>	
D0_SE<7>	B18	60	IPS8B	
--> un-used <--	D15	61	<space>	
CTRL0_SE	B19	62	IPS8B	
--> un-used <--	E15	63	<space>	
--> not connected <--	D17	64	{No pad}	chip
GND (GNDPY_P_6)	-	261	GNDPY	edge
GND (GNDCO_P_4)	-	261	GNDCO	1

Signal Name	Package Pin	Bonding land	pad type	
GND	-	261	CRNGNDPY(corner)	
GND (GNDCO_P_5)	-	261	GNDCO	chip
GND (GNDPY_P_7)	-	261	GNDPY	edge
D0_SE<6>	C18	65	IPS8B	
--> not connected <--	E16	66	{No pad}	
PARI0_SE	C19	67	IPS8B	
UP_DISC_P	F16	68	OPS0T	
--> un-used <--	D18	69	<space>	
--> un-used <--	F17	70	<space>	
--> un-used <--	E17	71	<space>	
D_OPP<0>	G16	72	OPS0T	
--> un-used <--	D19	73	<space>	
--> un-used <--	E18	74	<space>	
Vdd (+3.3V) (PWRPY_P_9)	-	277	PWRPY	
--> un-used <--	D20	75	<space>	
Vdd (+3.3V) (PWRCO_P_7)	-	277	PWRCO	
--> un-used <--	E19	76	<space>	
Vdd (+3.3V) (PWRPY_P_10)	-	277	PWRPY	
--> un-used <--	F18	77	<space>	
Vdd (+3.3V) (PWRCO_P_8)	-	277	PWRCO	
--> un-used <--	E20	78	<space>	
Vdd (+3.3V) (PWRPY_P_11)	-	277	PWRPY	
D_OPP<1>	G17	79	OPS0T	
GND (GNDCO_P_6)	-	262	GNDCO	
GND (GNDPY_P_8)	-	262	GNDPY	
NO_BOND_GNDCO_1			**GNDCO**	
--> un-used <--	F19	80	<space>	
D_OPP<5>	H16	81	OPS0T	
D_OPP<2>	G18	82	OPS0T	
D_OPP<6>	H17	83	OPS0T	
CLK_OPP	F20	84	OPS0T	
D_OPP<9>	J16	85	OPS0T	
D_OPP<3>	G19	86	OPS0T	
D_OPP<10>	J17	87	OPS0T	
D_OPP<7>	H18	88	OPS0T	
D_OPP<11>	J18	89	OPS0T	
D_OPP<4>	G20	90	OPS0T	
D_OPP<15>	K18	91	OPS0T	
D_OPP<8>	H19	92	OPS0T	
D_OPP<13>	K16	93	OPS0T	
D_OPP<12>	J19	94	OPS0T	
D_OPP<14>	K17	95	OPS0T	
D_OPP<16>	K19	96	OPS0T	
Vdd (+3.3V) (PWRPY_P_12)	-	278	PWRPY	
Vdd (+3.3V) (PWRCO_P_9)	-	278	PWRCO	
Vdd (+3.3V) (PWRPY_P_13)	-	278	PWRPY	
GND (GNDPY_P_9)	-	263	GNDPY	
GND (GNDCO_P_18)	-	263	GNDCO	

Signal Name	Package Pin	Bonding land	pad type	
D_OPP<18>	L17	97	OPS0T	
D_OPP<20>	L19	98	OPS0T	
D_OPP<17>	L16	99	OPS0T	
D_OPP<24>	M19	100	OPS0T	
D_OPP<19>	L18	101	OPS0T	
L_XFRM	N20	102	OPS0T	
D_OPP<23>	M18	103	OPS0T	
D_OPP<28>	N19	104	OPS0T	
D_OPP<22>	M17	105	OPS0T	
SOC_OPP	P20	106	OPS0T	
D_OPP<21>	M16	107	OPS0T	
D_OPP<27>	N18	108	OPS0T	
D_OPP<26>	N17	109	OPS0T	
PARI_OPP	P19	110	OPS0T	
D_OPP<25>	N16	111	OPS0T	
R_XFRM	R20	112	OPS0T	
GND (GNDPY_P_11)	-	264	GNDPY	
GND (GNDCO_P_7)	-	264	GNDCO	
D_OPP<31>	P18	113	OPS0T	
Vdd (+3.3V) (PWRCO_P_10)	-	279	PWRCO	
L_CCLK	R19	114	OPS0T	
Vdd (+3.3V) (PWRPY_P_14)	-	279	PWRPY	
--> un-used <--	T20	115	<space>	
Vdd (+3.3V) (PWRCO_P_11)	-	279	PWRCO	
--> un-used <--	R18	116	<space>	
Vdd (+3.3V) (PWRPY_P_15)	-	279	PWRPY	
--> un-used <--	T19	117	<space>	
Vdd (+3.3V) (PWRCO_P_12)	-	279	PWRCO	
--> un-used <--	U20	118	<space>	
Vdd (+3.3V) (PWRPY_P_16)	-	279	PWRPY	
--> un-used <--	T18	119	<space>	
--> un-used <--	U19	120	<space>	
D_OPP<30>	P17	121	OPS0T	↑
TXCC_P	T17	122	OPS0T	
D_OPP<29>	P16	123	OPS0T	
EMPT_CSTR_T	U18	124	OPS0T	
--> un-used <--	R17	125	<space>	
RESET_OPP(RES_OPP_P)	V19	126	OPS1T	
--> un-used <--	R16	127	<space>	
D_H_OPP<15>	V18	128	OPS1T	chip
GND (GNDPY_P_12)	-	265	GNDPY	edge
GND (GNDCO_P_8)	-	265	GNDCO	2

Signal Name	Package Pin	Bonding land	pad type	
GND	-	265	CRNGNDPY(corner)	
GND (GNDCO_P_9)	-	265	GNDCO	chip
GND (GNDCO_P_10)	-	265	GNDCO	edge
GND (GNDPY_P_13)	-	265	GNDPY	3
--> not connected <--	U17	129	{no pad}	
--> not connected <--	T16	130	{no pad}	
--> un-used <--	W19	131	<space>	
--> un-used <--	T15	132	<space>	
D_H_OPP<12>	W18	133	OPS1T	
--> un-used <--	U15	134	<space>	
D_H_OPP<14>	V17	135	OPS1T	
C_CLK_TAP<3>	T14	136	IPS8B	
--> un-used <--	U16	137	<space>	
D_H_OPP<13>	W17	138	OPS1T	
Vdd (+3.3V) (PWRPY_P_17)	-	280	PWRPY	
D_H_OPP<11>	V16	139	OPS1T	
Vdd (+3.3V) (PWRCO_P_13)	-	280	PWRCO	
D_H_OPP<10>	W16	140	OPS1T	
Vdd (+3.3V) (PWRPY_P_18)	-	280	PWRPY	
D_H_OPP<9>	X16	141	OPS1T	
Vdd (+3.3V) (PWRCO_P_14)	-	280	PWRCO	
D_H_OPP<6>	V15	142	OPS1T	
Vdd (+3.3V) (PWRPY_P_19)	-	280	PWRPY	
D_H_OPP<7>	W15	143	OPS1T	
GND (GNDCO_P_11)	-	266	GNDCO	
GND (GNDPY_P_14)	-	266	GNDPY	
NO_BOND_GNDCO_4			**GNDCO**	
--> un-used <--	U14	144	<space>	
C_CLK_TAP<2>	T13	145	IPS8B	
D_H_OPP<8>	X15	146	OPS1T	
--> un-used <--	U13	147	<space>	
D_H_OPP<5>	V14	148	OPS1T	
C_CLK_TAP<1>	T12	149	IPS8B	
D_H_OPP<3>	W14	150	OPS1T	
--> un-used <--	U12	151	<space>	
D_H_OPP<4>	X14	152	OPS1T	
SOC_H_OPP	V12	153	OPS1T	
D_H_OPP<1>	V13	154	OPS1T	
--> un-used <--	V11	155	<space>	
D_H_OPP<2>	W13	156	OPS1T	
C_CLK_TAP<0>	T11	157	IPS8B	
--> un-used <--	X13	158	<space>	
--> un-used <--	U11	159	<space>	
D_H_OPP<0>	W12	160	OPS1T	
Vdd (+3.3V) (PWRPY_P_20)	-	281	PWRPY	
Vdd (+3.3V) (PWRCO_P_15)	-	281	PWRCO	
Vdd (+3.3V) (PWRPY_P_21)	-	281	PWRPY	
NO_BOND_PWRCO_2			**PWRCO**	
GND (GNDCO_P_14)	-	267	GNDCO	
GND (GNDPY_P_16)	-	267	GNDPY	

Signal Name	Package Pin	Bonding land	pad type
D_L_OPP<13>	U10	161	OPS1T
DAV_H_OPP	W11	162	OPS1T
CLR_ERR	T10	163	IPS8B
D_L_OPP<15>	W10	164	OPS1T
D_L_OPP<14>	V10	165	OPS1T
D_L_OPP<12>	W9	166	OPS1T
D_L_OPP<11>	V9	167	OPS1T
D_L_OPP<10>	W8	168	OPS1T
TIME_SYNC(T_SYNC)	U9	169	IPS8B
D_L_OPP<8>	X7	170	OPS1T
RESET	T9	171	IPS8B
D_L_OPP<9>	V8	172	OPS1T
--> un-used <--	U8	173	<space>
D_L_OPP<7>	W7	174	OPS1T
CELL_CLK	T8	175	IPS8B
D_L_OPP<5>	X6	176	OPS1T
GND (GNDCO_P_12)	-	268	GNDCO
GND (GNDPY_P_17)	-	268	GNDPY
D_L_OPP<6>	V7	177	OPS1T
NO_BOND_GNDCO_5			**GNDCO**
Vdd (+3.3V) (PWRPY_P_22)	-	282	PWRPY
D_L_OPP<4>	W6	178	OPS1T
Vdd (+3.3V) (PWRCO_P_16)	-	282	PWRCO
D_L_OPP<2>	X5	179	OPS1T
Vdd (+3.3V) (PWRPY_P_23)	-	282	PWRPY
D_L_OPP<3>	V6	180	OPS1T
Vdd (+3.3V) (PWRCO_P_17)	-	282	PWRCO
D_L_OPP<1>	W5	181	OPS1T
Vdd (+3.3V) (PWRPY_P_24)	-	282	PWRPY
SOC_L_OPP	X4	182	OPS1T
Vdd (+3.3V) (PWRCO_P_18)	-	282	PWRCO
D_L_OPP<0>	V5	183	OPS1T
--> un-used <--	W4	184	<space>
--> un-used <--	U7	185	<space>
--> un-used <--	U5	186	<space>
CLK(C_P)	T7	187	IPS8B
DAV_L_OPP	V4	188	OPS1T
--> un-used <--	U6	189	<space>
--> un-used <--	W3	190	<space>
--> un-used <--	T6	191	<space>
--> not connected <--	V3	192	{No pad}
GND (GNDPY_P_18)	-	269	GNDPY
GND (GNDCO_P_13)	-	269	GNDCO

chip edge 3

Signal Name	Package Pin	Bonding land	pad type	
GND	-	269	CRNGNDPY(Corner)	
--> No bond land needed <--	-	-	MISOPYR	chip
GND (MGNDCO_P_1)	-	269	MGNDCO	edge
GND (MGNDPY_P_1)	-	269	MGNDPY	
--> not connected <--	U4	193	{No pad}	
WIDTH_LINK	T5	194	MIPS8G	
--> un-used <--	W2	195	<space>	
TCA_LINK	R5	196	MIPS8G	
PAD_ZERO(P_ZERO)	V2	197	MIPS8G	
TCA_FF_LINK	R4	198	MIPS8G	
Vcc(+5V) (MPWRPY_P_1)	U3	199	MPWRPY	
UNASSIGN_EN(UN_EN_P)	P5	200	MIPS8G	
CLK_LINK	T4	201	MIPS8G	
--> No bond land needed <--	-	-	MIPSOPYL	
FSL_LEN_P_0	U2	202	OPS0T	
Vdd (+3.3V) (PWRCO_P_19)	-	283	PWRCO	
FSL_LEN_P_1	T3	203	OPS0T	
Vdd (+3.3V) (PWRPY_P_25)	-	283	PWRPY	
FSL_LEN_P_2	U1	204	OPS0T	
Vdd (+3.3V) (PWRCO_P_20)	-	283	PWRCO	
FSL_LEN_P_3	T2	205	OPS0T	
Vdd (+3.3V) (PWRCO_P_21)	-	283	PWRCO	
FSL_LEN_P_4	R3	206	OPS0T	
Vdd (+3.3V) (PWRCO_P_22)	-	283	PWRCO	
FSL_LEN_P_5	T1	207	OPS0T	
Vdd (+3.3V) (PWRPY_P_27)	-	283	PWRPY	
FSL_LEN_P_6	P4	208	OPS0T	
GND (GND_PY__21)	-	270	GNDPY	
GND (GNDCO_P_15)	-	270	GNDCO	
FSL_LEN_P_7	R2	209	OPS0T	
TLDC_P	N5	210	OPS0T	
CS1_OCC_P_7	P3	211	OPS0T	
CS1_OCC_P_6	N4	212	OPS0T	
CS1_OCC_P_5	R1	213	OPS0T	
CS1_OCC_P_4	M5	214	OPS0T	
CS1_OCC_P_3	P2	215	OPS0T	
CS1_OCC_P_2	M4	216	OPS0T	
CS1_OCC_P_1	N3	217	OPS0T	
CS1_OCC_P_0	M3	218	OPS0T	
CS0_OCC_P_7	P1	219	OPS0T	
CS0_OCC_P_6	L3	220	OPS0T	
CS0_OCC_P_5	N2	221	OPS0T	
CS0_OCC_P_4	L5	222	OPS0T	
CS0_OCC_P_3	M2	223	OPS0T	
CS0_OCC_P_2	L4	224	OPS0T	
GND (GND_PY_22)	-	271	GNDPY	
GND (GNDCO_P_16)	-	271	GNDCO	
Vdd (+3.3V) (PWRPY_P_28)	-	284	PWRPY	
Vdd (+3.3V) (PWRCO_P_26)	-	284	PWRCO	
Vdd (+3.3V) (PWRCO_P_25)	-	284	PWRCO	

Signal Name	Package Pin	Bonding land	pad type
CS0_OCC_P_1	L2	225	OPS0T
CS0_OCC_P_0	K4	226	OPS0T
TEST_EN	K2	227	IPS8B
--> un-used <--	K5	228	<space>
[missing]TEST_IN2	J2	229	IPS8B
[missing]TEST_IN1	K3	230	IPS8B
--> un-used <--	H1	231	<space>
[missing]TEST_IN0	J3	232	IPS8B
BIST_CLK	H2	233	IPS8B
--> un-used <--	J4	234	<space>
BIST_TEST	H3	235	IPS8B
BIST_RES0	J5	236	OPS0T
BIST_RES1	G1	237	OPS0T
BIST_RES2	H4	238	OPS0T
--> un-used <--	G2	239	<space>
--> un-used <--	H5	240	<space>
--> un-used <--	G3	241	<space>
GND (GNDCO_P_17)	-	272	GNDCO
GND (GNDPY_P_19)	-	272	GNDPY
--> un-used <--	F1	242	<space>
Vdd (+3.3V) (PWRCO_P_24)	-	285	PWRCO
--> un-used <--	F2	243	<space>
Vdd (+3.3V) (PWRCO_P_29)	-	285	PWRCO
NO_BOND_GNDCO_3			**GNDCO**
NO_BOND_PWRCO_1			**PWRCO**
--> un-used <--	F3	244	<space>
Vdd (+3.3V) (PWRCO_P_27)	-	285	PWRCO
--> un-used <--	E1	245	<space>
Vdd (+3.3V) (PWRPY_P_26)	-	285	PWRPY
--> un-used <--	E2	246	<space>
--> un-used <--	E3	247	<space>
--> un-used <--	G4	248	<space>
--> un-used <--	D2	249	<space>
--> un-used <--	G5	250	<space>
--> un-used <--	D3	251	<space>
--> un-used <--	F4	252	<space>
D3_SE<1>	C2	253	IPS8B
--> un-used <--	E4	254	<space>
D3_SE<0>	B2	255	IPS8B
--> un-used <--	F5	256	<space>
GND (GNDPY_P_20)	D4	257	GNDPY
GND (GNDCO_P_19)	-	273	GNDCO

chip edge 4

Appendix B

(Copy of 299 PGA pin out from data book)
(A single page, page 35 of data book)

Appendix C

(Copy of Bonding Diagrams Submitted to Atmel/ES2)
(4 pages)

The package used for the OPP chip is a 299 pin PGA package with an internal power and ground plane. The use of the power and ground planes in the package force a fixed package pin assignment for the package power and ground outside pins. Inside the bond cavity, the power and the ground planes each appear as fixed location bond land *regions* around the bond cavity. These bonding regions vary in size from an area large enough to support bonds to seven power or ground chip pads, to an area the same size as the signal bonding lands. Also, the placement of a power or ground pad around any part of the periphery of the chip that is not lined up with the appropriate power or ground region can not be effectively fed from the package. The inductance of a signal pin circuit is so much higher than the inductance of a power or ground plane connection circuit that there is little value in making a power or ground connection using a signal pin circuit. However, to effectively feed the core circuit from the pad ring power, it is often helpful to place a power or ground pad in the pad ring and use this pad to only feed power to the core. Thus chip designs end up with power and ground pads that are not intended to be bonded. The Atmel/ES2 software tool set does not support this package very well. Thus there is some hand drawn work required to complete the bonding diagrams. To assure there are no errors in the hand drawn work, there are four pages of bonding diagrams.

The four pages of bonding diagrams are attached as this Appendix C. The first page details the extent of the hand work, and points out the core power feed pads on the chip that do not receive bond wires. The second page shows all the bonds on one diagram. Page two is a repeat of page one without all the notes. The package cavity is a two tier design. The bond connections to just the bottom(inside) tier is shown on the third page, and the bonds to just the top (outer) tier is shown on page four.

TO BE ADDED

ADDITIONS, Version 0.2

- Signal CLK_OPP was added sometime. Not sure this signal was in the Aug, ’96 version.
- BIST_TEST and BIST_CLK were added sometime. Not sure these signals were in the Aug. ’96 version.
- added TIME_SYNC and PAD_ZERO signals
- Changed QUICK_TEST3 to TEST_EN
- Changed QUICK_TEST< 2 . .0 > to TEST_IN < 2 . . 0 >