The Syndicated®
A Technical Newsletter for FPGA, ASIC Verification, and DSP Designers

Q4, 2006

Adaptive Control of FPGA Computation with Thermal Feedback

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http://www.arl.wustl.edu/projects/fpx/reconfig.htm

High performance applications implemented with FPGAs can generate more heat than what their package can dissipate. This article overviews thermal results obtained from programming applications into a Xilinx Virtex FPGA. It also describes how a thermally adaptive computational mechanism was implemented that modulates the frequency to an FPGA circuit as a function of the temperature of the device. Both simple benchmark circuits and a more complex image processing circuit were implemented using the Synplicity® Synplify® Pro tool.

Hardware Deployment Configuration

A Field-programmable Port Extender (FPX) module was mounted in a 3U rack-mount chassis to evaluate how effective thermally-adaptive circuits could achieve in a realistic deployment configuration. This case was equipped with 2 fans that each supplied 250 Linear Feet per Minute (LFM) of air flow through the chassis. The system has a cover which was removed for the photo shown below in Figure 1

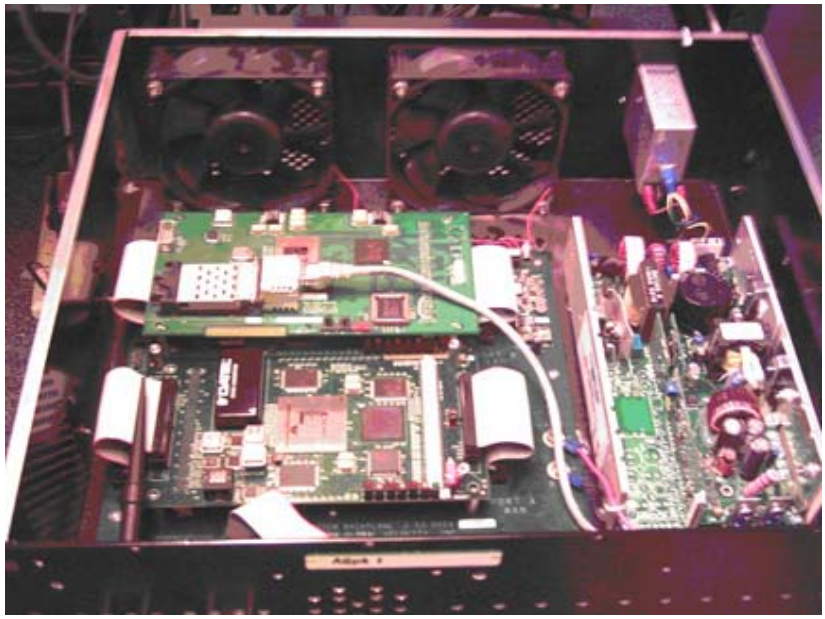

Figure 1. Experimentation Setup

FPGA Thermal Characterization

The structure of a basic benchmark circuit used to generate circuits that uniformly generated heat across an FPGA is shown in Figure 2. This circuit was complied from VHDL that included Relative Location (RLOC) constraints using the Synplify Pro software. The RLOC constraints allowed

the precise placement of Lookup Table (LUT) and Delay Flip/Flop (DFF) components uniformly across the device and allowed us to systematically scale this computational structure to create benchmark circuits that consume increasing amounts of power. Careful placement of the components allowed us to built benchmark circuits that consumed nearly 100% of the FPGA logic resources and operated at a frequency of 400 MHz. [FPL'06].

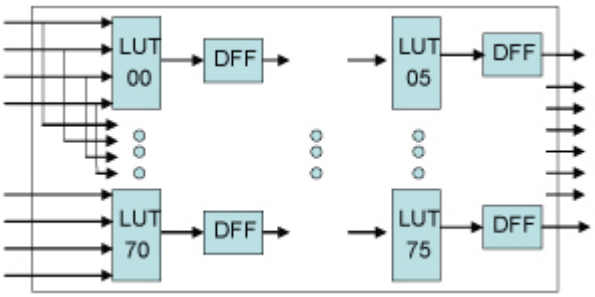

Figure 2: Basic Structure of Thermal Benchmark Circuits

Thermally Adaptive Computing Mechanism

We implemented the thermally adaptive computing mechanism using the FPX platform [EHW'01]. Figure 3 shows the relevant components of the FPX and the major components of our thermal feedback controller. We configured our benchmark application circuit into the VirtexE-2000 FPGA on the FPX platform called the Reconfigurable Application Device (RAD). We programmed the Thermal Feedback Frequency Controller into the VirtexE-600 FPGA on the FPX platform called the Network Interface Device (NID).

We used a MAX-1618 analog sensor to monitor the current passing through the thermal diode on the RAD. The digitized value of the temperature was monitored by the Thermal Feedback controller on the NID which in turn controlled the frequency of the application circuit that ran on the RAD.

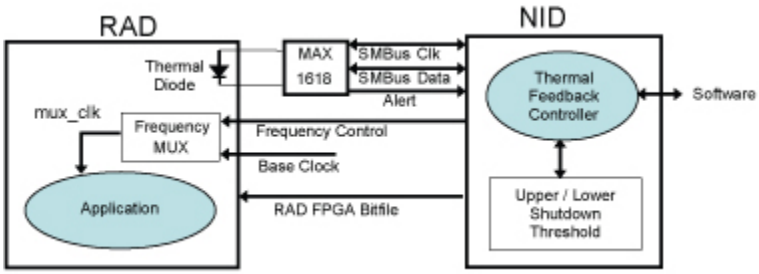

Figure 3: Modules on the FPX for Thermally Adaptive Computing

Our thermal feedback controller modulated a frequency multiplexer signal that provided the application circuit with either a slow clock (1X) or a fast clock (4x). As the junction temperature on the RAD changed, the feedback control circuit compared the value to an upper and lower temperature threshold programmed into the registers on the NID. Thresholds were chosen so as to maintain a target average temperature on the RAD within a tight bound. When the temperature hit the upper temperature, the frequency was decreased but when the temperature fell below the lower threshold, the frequency was increased by a factor of 4. By operating our circuit exactly at the highest-possible safe temperature, our circuit was able to achieve maximum computational performance.

Results

We first tested the simple benchmark circuits, we determined that the Xilinx VirtexE-2000 device used in our study without a heatsink exceeded it's thermal shut down threshold when: over 50% of the logic resources were fully utilized, the FPGA was operated at 100 MHz, and the circuit data forced data transitions on every clock cycle [FPL'06].

We next implemented a complex image processing application. Careful placement of logic enabled us to pack 20% more logic into the FPGA as compared to a placement that did not use RLOC constraints. The circuit achieved timing closure so as to enable operating the application at over 100 Megahertz, but was not able to sustain that performance with certain data patterns that caused a large number of transitions. The circuit would overheat with certain data patterns that caused a large number of transitions within the device.

By using the thermal feedback controller to modulate the application circuit's frequency as a function of junction temperature, the resulting image processing application circuit was able to outperform a non-adaptive application that only used a fixed thermal shutdown threshold by a factor of 2.4. Details of the experiments are provided in a full-length paper that appears in the Field Programmable Technology conference [FPT'06].

References

[EHW'01] Evolvable Internet Hardware Platforms, by John W. Lockwood, NASA/DoD Workshop on Evolvable Hardware, Long Beach, CA, July 12-14, 2001, pp. 271-279.

[FPL'06] "A Thermal Management and Profiling Method for Reconfigurable Hardware Applications", by Phillip H. Jones, John W. Lockwood, and Young H. Cho; Field Programmable Logic and Applications (*FPL'06*), Madrid, Spain, Aug, 2006.

[FPT'06] "An Adaptive Frequency Control Mechanism using Thermal Feedback for Reconfigurable Hardware Applications", by Phillip H. Jones, Young H. Cho, and John W. Lockwood; Field Programmable Technology (*FPT'06*), Bangkok, Thailand, Dec. 2006