Statistics Module

Abdel Rigumye {ar1}@ar1.wustl.edu
Washington University, St.Louis, MO

A. Statistics Module

The Statistics Module can be seen in Figure 1. Internally, it is composed of four instantiations of the StatMod [1] circuit described in subsection 1. The first instantiation stores a count of packets. The second instantiation accumulates the SendDelay field of the game header. The third instantiation stores the move count. The fourth stores a set of counters, where each entry counts the occurrence of a NetEvent Object.

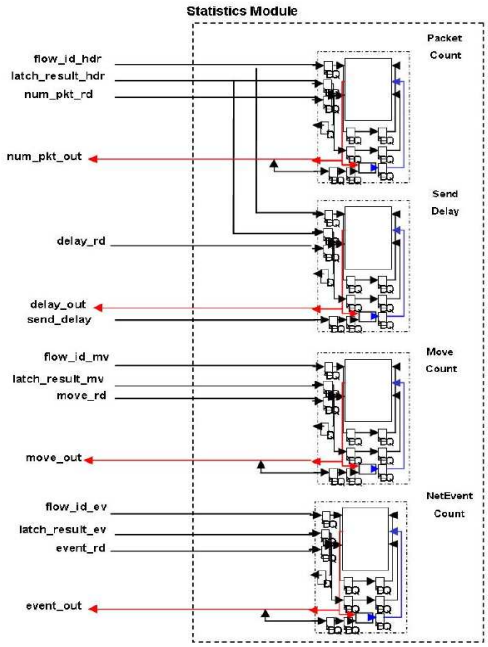

Fig. 1. Statistics Module Circuit Diagram

1) StatMod: The Statistics Module provides a way to aggregate statistics in FPGA hardware. This circuit shown in Figure 2 allows us to store and update up to 256 different counters stored in block RAM.

The following processing sequence occurs when updating statistics stored in this module:

- The *flowid* and *latchresult* signals from the Processing Modules, are used to address a location in block RAM and initiate a read respectively;
- The read value, *paraminput* signal, *flowid*, and *latchresult* signals propagate through a two stage pipeline;
- In this pipeline the read value is added to the *paraminput* signal;
- Leaving this pipeline, the sum is written into the original location addressed by the *flowid* signal. This write is initiated by the *latchresult* signal;

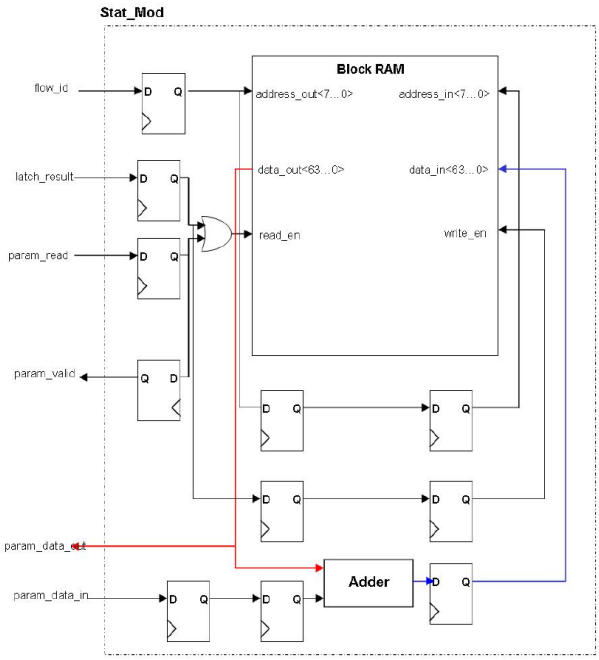

Fig. 2. StatMod Circuit Diagram

This module provides a simple interface that the Control Processor uses to access stored statistics. By asserting the *paramread* signal, the block RAM entry addressed by *flowid* is returned accompanied by a *paramvalid* signal.

REFERENCES

[1] J. Attig, Micheal; Lockwool, “Usage of the Statistics Counter Plus Component in Networking Hardware Modules.”