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FPGA platform fuels study of reconfigurable networks

By Ron Wilson

SAN MATEO, CALIF. – An on-the-fly reconfigurable hardware platform and a library of networking application modules form the basis for continuing research into OC-48 wire-speed network processing at Washington University (St. Louis). The Port Extender platform plugs into the backplane of a conventional network switch to add applications.

"We originally developed Port Extender to investigate computing needs for quality of service," said John Lockwood, assistant professor of computer science at Washington University. The device is a plug-in card carrying a pair of Xilinx Virtex FPGAs that can be programmed either via incoming traffic on the router or from each other. In the latter mode, one of the FPGAs can be altered in as little as 20 ms.

Modules developed

Hardware modules are loaded into the FPGAs to add features to the switch. Researchers have developed modules to implement a round-robin scheduling algorithm with approximately 2-Gbit/second traffic loads, fast routing tables, data compression and video recoding. This has allowed research into not only the routing issues involved in QoS design, but also content-specific compression and related topics.

Lockwood said the team has developed a scheduler/loader program that runs in one of the FPGAs to manage the swappable modules. This would permit the parts to add and drop features in response to changing traffic flows without reliance on an external control plane processor.

Port Extender and work done with it are documented at *www.arl.wustl.edu/arl/projects/fpx/*.